

# Automotive 500 mA, High PSRR Low I<sub>Q</sub> LDO

## ■ Features

- AEC-Q100 qualified:
  - Device ambient temperature:  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
  - Device junction temperature:  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$
- Operating input voltage range: 1.65 V to 5.5 V
- Available in various fixed voltage options: 1 V to 3.3 V
- Ultra-high PSRR and low noise:
  - PSRR: 95 dB (typ.) at  $f = 1\text{ kHz}$
  - Noise: 20  $\mu\text{V}_{\text{RMS}}$
- Low quiescent current:
  - 18  $\mu\text{A}$  typical at no load
  - 10 nA shutdown current
- $\pm 2\%$  output voltage accuracy over temperature
- Stable with a 1  $\mu\text{F}$  small case size ceramic capacitor
- Quick output discharge:
  - DIA7965A: available
  - DIA7965B: not available

## ■ Applications

- Automotive camera and radar
- Automotive infotainment
- Telematics systems
- Navigation systems
- Automotive audio

## ■ Package Information

Part Number	Package	Body Size
DIA7965	SOT23-5	2.9 mm × 1.6 mm
	DFN-4	1 mm × 1 mm

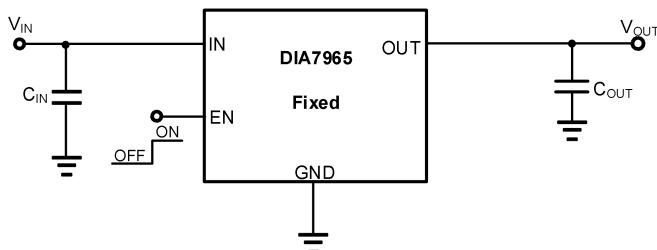
## ■ Description

The DIA7965 series is a 500 mA, ultra-high Power Supply Ripple Rejection (PSRR) low dropout CMOS linear regulator. The device features ultra-high PSRR and low noise to meet the requirements of RF and other sensitive analog circuits in automotive applications.

The DIA7965 operates an input voltage range of 1.65 V to 5.5 V and supports fixed output voltage from 1 V to 3.3 V. With 18  $\mu\text{A}$  low quiescent current at no load, the DIA7965 is quite suitable for systems requiring low power and provides fast line and load transient performance.

The DIA7965 is stable with an 1  $\mu\text{F}$  input and an 1  $\mu\text{F}$  output small ceramic capacitor, allowing for a small overall solution size. A precision band-gap and error amplifier provide high accuracy of  $\pm 2\%$  over operating temperature range. The DIA7965 is available in SOT23-5 and tiny DFN1\*1-4 packages.

## ■ Simplified Schematic



## ■ Ordering Information

Ordering Part Number	Top Marking	MSL	Description	RoHS	T <sub>A</sub>	Package	
DIA7965AaaST5	AEXYW	1	Active discharge	Green	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIA7965BaaST5	AFXYW	1	Non-active discharge	Green	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIA7965AaaEN4	YWEX	1	Active discharge	Green	-40 to 125°C	DFN1*1-4	Tape & Reel, 10000
DIA7965BaaEN4	YWFX	1	Non-active discharge	Green	-40 to 125°C	DFN1*1-4	Tape & Reel, 10000

### Output Voltage Options

Option Code "aa"	10	11	12	15	18	25	28	29	30	33
Voltage (V)	1.0	1.1	1.2	1.5	1.8	2.5	2.8	2.9	3	3.3

### Marking Definition

AEXYW	AE: product code; Y: year code; W: week code
AFXYW	AF: product code; Y: year code; W: week code
YWEX	Y: year code; W: week code; E: product code
YWFX	Y: year code; W: week code; F: product code

### Voltage Code

Option Code "X"	E	D	F	G	H	J	K	R	L	M
Voltage (V)	1.0	1.1	1.2	1.5	1.8	2.5	2.8	2.9	3	3.3

If you encounter any issue in the process of using the device, please contact our customer service at [marketing@dioo.com](mailto:marketing@dioo.com) or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at [docs@dioo.com](mailto:docs@dioo.com). Your feedback is invaluable for us to provide a better user experience.

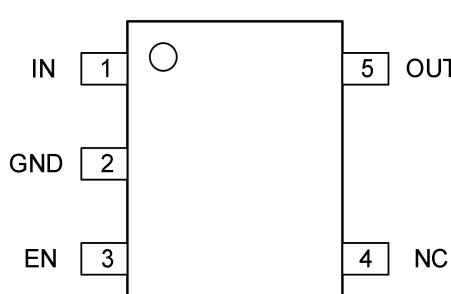
## Table of Contents

1. Pin Assignment and Functions .....	1
2. Absolute Maximum Ratings .....	1
3. Recommended Operating Conditions .....	2
4. ESD Ratings .....	2
5. Thermal Considerations .....	2
6. Electrical Characteristics .....	3
7. Typical Characteristic .....	4
8. Block Diagram .....	7
9. Function Description .....	8
9.1. Input capacitor selection ( $C_{IN}$ ) .....	8
9.2. Output capacitor selection ( $C_{OUT}$ ) .....	8
9.3. Enable operation .....	8
9.4. Output current limit .....	9
9.5. Short circuits protection .....	9
9.6. Thermal shutdown .....	9
9.7. Dropout voltage .....	9
9.8. Power dissipation and heat sinking .....	9
9.9. Power supply rejection ratio .....	10
9.10. Turn-on time .....	10
10. Layout Guidelines .....	10
11. Physical Dimensions .....	11
11.1. SOT23-5 .....	11
11.2. DFN1*1-4 .....	12

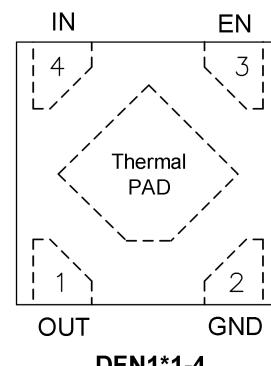
## List of Figures

Figure 1. Output voltage (1.2 V) vs. Temperature .....	4
Figure 2. Output voltage (1.8 V) vs. Temperature .....	4
Figure 3. Output voltage (3.3 V) vs. Temperature .....	4
Figure 4. Dropout voltage vs. Output current .....	4
Figure 5. PSRR vs. Frequency .....	4
Figure 6. PSRR vs. Frequency .....	4
Figure 7. PSRR vs. Frequency .....	5
Figure 8. PSRR vs. Frequency .....	5
Figure 9. Turn-on time .....	5
Figure 10. Turn-off time .....	5
Figure 11. Load transient response .....	5
Figure 12. Load transient response .....	5
Figure 13. Load transient response .....	6
Figure 14. Load transient response .....	6
Figure 15. Shutdown current vs. Input voltage .....	6
Figure 16. Shutdown current vs. Temperature .....	6
Figure 17. Enable current vs. Input voltage .....	6
Figure 18. Quiescent current vs. Input voltage .....	6
Figure 19. Quiescent current vs. Temperature .....	7
Figure 20. Dropout voltage vs. Temperature .....	7

## 1. Pin Assignment and Functions



SOT23-5



DFN1\*1-4

Top view

Pin Name	Description
IN	Input voltage supply pin.
GND	Power supply ground.
EN	Enable pin. This pin has a 100 nA pull-down current source. Connect to logic high for normal operation.
NC	Do not connect.
OUT	Regulated output voltage. Bypassed the output with a small 1 $\mu$ F ceramic capacitor.
Thermal PAD	Exposed Pad. Exposed pad can be tied to ground plane for better power dissipation.

## 2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
$V_{IN}$	Input voltage	-0.3 V to 6	V
$V_{OUT}$	Output voltage	-0.3 to $V_{IN} + 0.3$ , max.6	V
$V_{EN}$	Chip enable input	-0.3 to 6	V
$t_{sc}$	Output short circuit duration	unlimited	s
$T_J$	Maximum junction temperature	150	°C
$T_{STG}$	Storage temperature	-65 to 150	°C

### 3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	Input voltage	1.65 to 5.5	V
T <sub>A</sub>	Operating free-air temperature	-40 to 125	°C

### 4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Parameter	Standard	Value	Unit
ESD	Human-body model (HBM), per AEC Q100-002, all pins	±7000	V
	Charged device model (CDM), per AEC Q100-01, all pins	±2000	V

### 5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	Value	Unit
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	SOT23-5	218.2
		DFN1*1-4	198

## 6. Electrical Characteristics

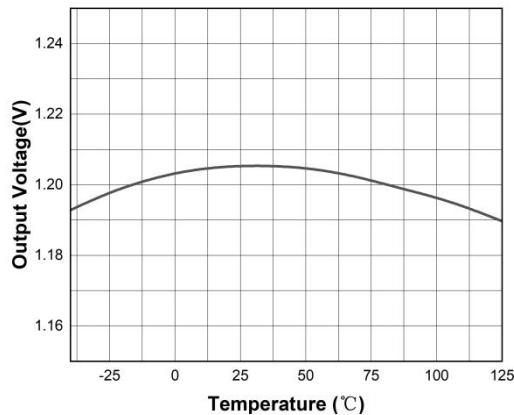
The typical values are obtained under these conditions unless otherwise specified:  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ ;  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ . Typical values are at  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{IN}$	Operating input voltage			1.65		5.5	V
$V_{OUT}$	Output voltage accuracy	$V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ , $I_{OUT} = 1\text{ mA}$	$V_{OUT} < 2\text{ V}$	-40		40	mV
			$V_{OUT} \geq 2\text{ V}$	-2		2	%
$Line_{Reg}$	Line regulation	$V_{OUT(NOM)} + 1\text{ V} < V_{IN} \leq 5.5\text{ V}$				6	mV
$Load_{Reg}$	Load regulation	$I_{OUT} = 1\text{ mA}$ to $500\text{ mA}$				40	mV
$V_{DO}$	Dropout voltage	$I_{OUT} = 500\text{ mA}$	$V_{OUT(NOM)} = 1.8\text{ V}$		290	370	mV
			$V_{OUT(NOM)} = 2.8\text{ V}$		180	270	
			$V_{OUT(NOM)} = 3.3\text{ V}$		160	260	
$I_{CL}$	Output current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$		500	700		mA
$I_{SC}$	Short circuit current	$V_{OUT} = 0\text{ V}$			200		mA
$I_Q$	Quiescent current	$I_{OUT} = 0\text{ mA}$			18	55	$\mu\text{A}$
$I_{SD}$	Shutdown current	$V_{EN} = 0.4\text{ V}$ , $V_{IN} = 5\text{ V}$			0.01	20	$\mu\text{A}$
$V_{ENH}$	EN pin threshold voltage	EN input voltage high		1			V
$V_{ENL}$		EN input voltage low				0.4	V
$I_{EN}$	EN pull down current	$V_{EN} = 5\text{ V}$			0.1	0.5	$\mu\text{A}$
$t_{ON}$	Turn-on time	$C_{OUT} = 1\text{ }\mu\text{F}$ , from assertion of $V_{EN}$ to $V_{OUT} = 90\% V_{OUT(NOM)}$			300		$\mu\text{s}$
$PSRR$	Power supply rejection ratio	$I_{OUT} = 10\text{ mA}$	$f = 100\text{ Hz}$		91		dB
			$f = 1\text{ kHz}$		95		
			$f = 10\text{ kHz}$		75		
			$f = 100\text{ kHz}$		55		
			$f = 1\text{ MHz}$		56		
$V_N$	Output voltage noise	$f = 10\text{ Hz}$ to $100\text{ kHz}$	$I_{OUT} = 1\text{ mA}$		20		$\mu\text{V}_{\text{RMS}}$
			$I_{OUT} = 500\text{ mA}$		15		
$R_{DIS}$	Active output discharge resistance	$V_{EN} = 0.4\text{ V}$ , DIA7965A only		50	100	150	$\Omega$
$T_{SDH}$	Thermal shutdown threshold	Temperature rising			160		$^\circ\text{C}$
$T_{SDL}$		Temperature falling			135		$^\circ\text{C}$

### Note:

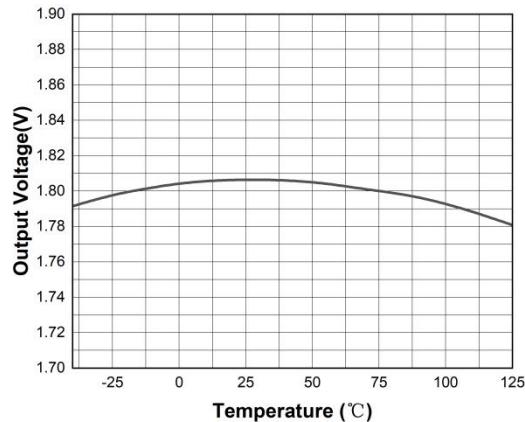
(1) Specifications subject to change without notice.

## 7. Typical Characteristic



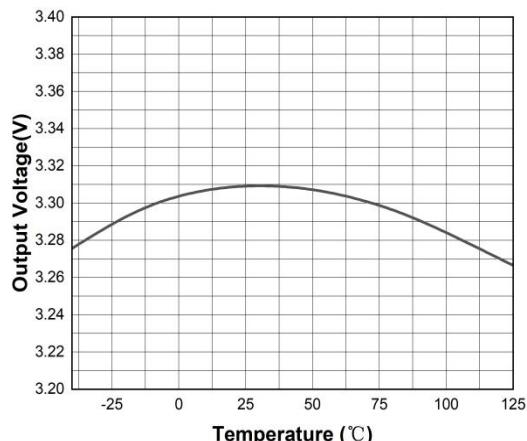
$V_{OUT} = 1.2 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$

Figure 1. Output voltage (1.2 V) vs. Temperature



$V_{OUT} = 1.8 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$

Figure 2. Output voltage (1.8 V) vs. Temperature



$V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$

Figure 3. Output voltage (3.3 V) vs. Temperature

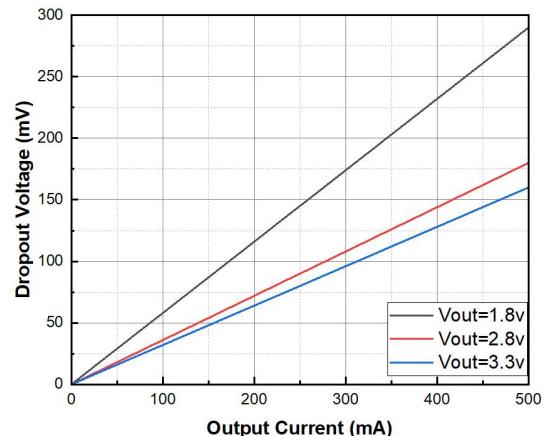
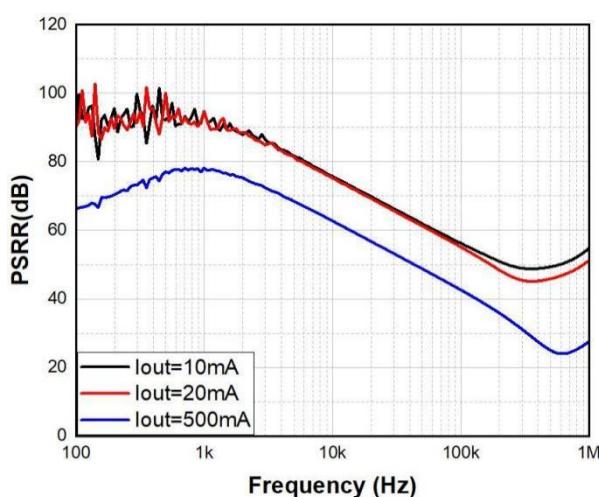
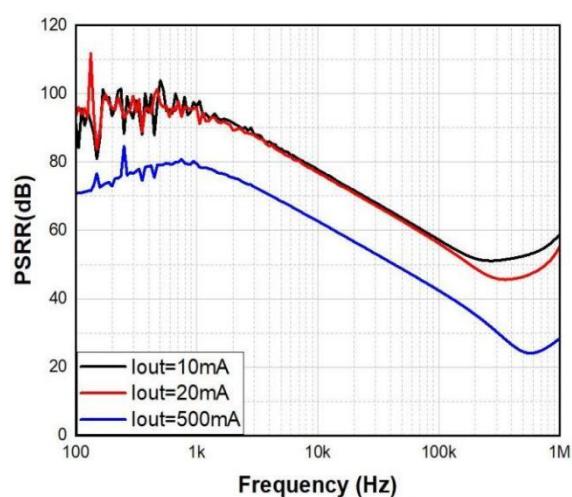


Figure 4. Dropout voltage vs. Output current



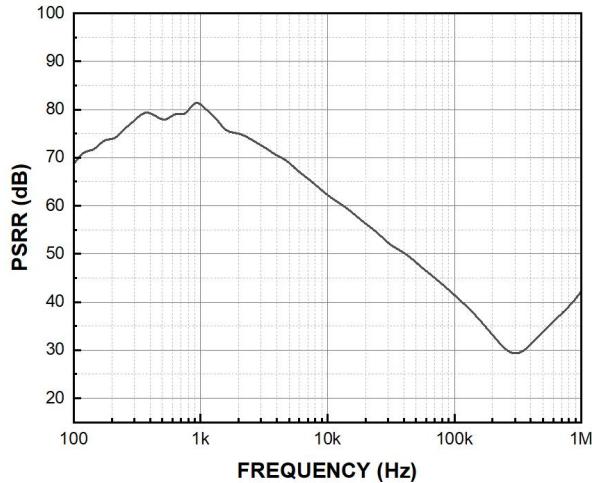
$V_{IN} = 2.2 \text{ V} + 200 \text{ mV}_{PP}$ ,  $V_{OUT} = 1.2 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$

Figure 5. PSRR vs. Frequency



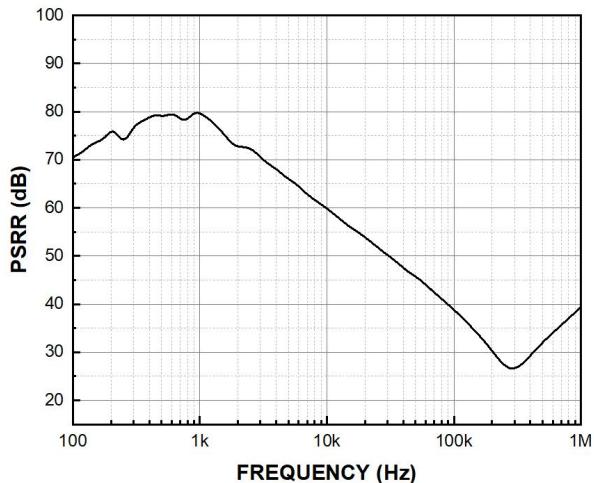
$V_{IN} = 4.3 \text{ V} + 200 \text{ mV}_{PP}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$

Figure 6. PSRR vs. Frequency



$V_{IN} = 3.3 \text{ V} + 0.1V_{PP}$ ,  $V_{OUT} = 2.8 \text{ V}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  
 $I_{OUT} = 250 \text{ mA}$

Figure 7. PSRR vs. Frequency



$V_{IN} = 3.8 \text{ V} + 0.1V_{PP}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  
 $I_{OUT} = 250 \text{ mA}$

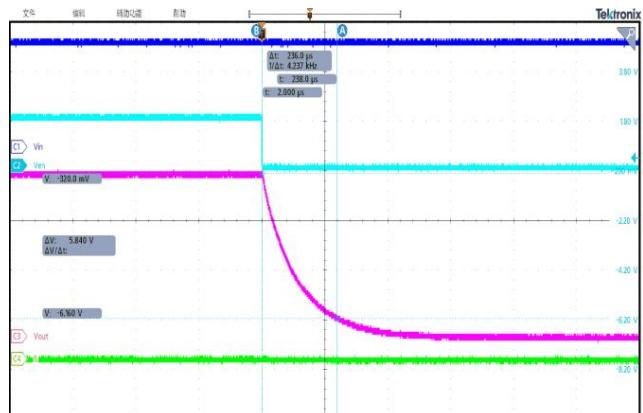
Figure 8. PSRR vs. Frequency



$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $I_L = 1 \text{ mA}$

From assertion of  $V_{EN}$  to  $V_{OUT} = 90\% V_{OUT(NOM)}$

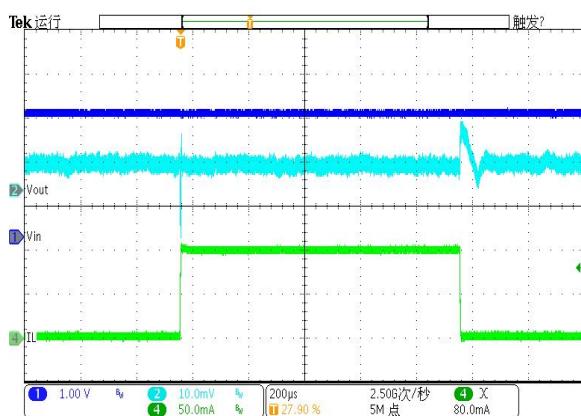
Figure 9. Turn-on time



$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $I_L = 1 \text{ mA}$

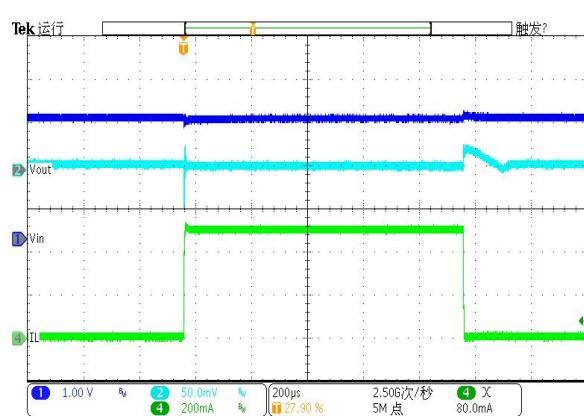
From assertion of  $V_{EN}$  to  $V_{OUT} = 0$

Figure 10. Turn-off time



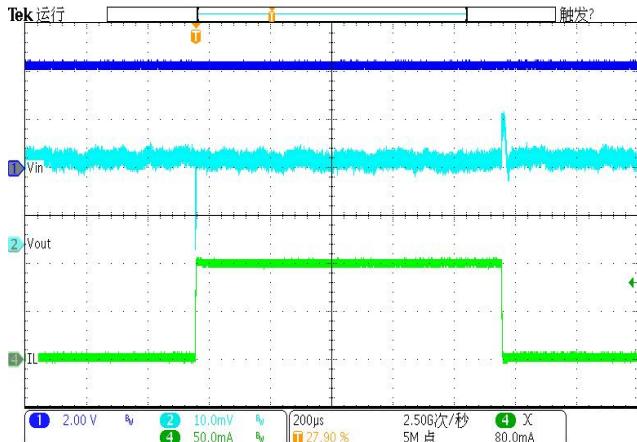
$V_{IN} = 2.8 \text{ V}$ ,  $V_{OUT} = 1.8 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$  to  $100 \text{ mA}$

Figure 11. Load transient response



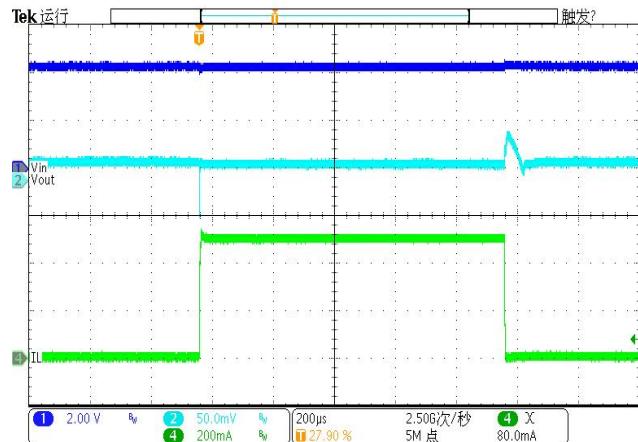
$V_{IN} = 2.8 \text{ V}$ ,  $V_{OUT} = 1.8 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$  to  $500 \text{ mA}$

Figure 12. Load transient response



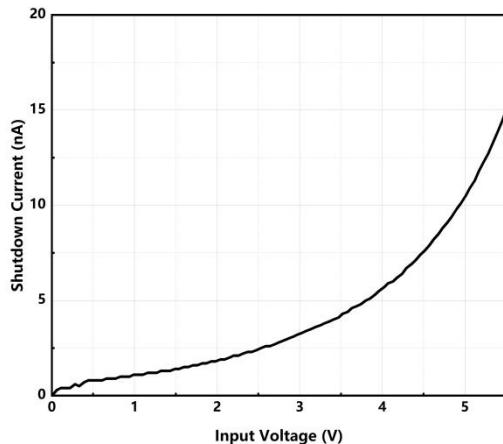
$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$  to  $100 \text{ mA}$

Figure 13. Load transient response



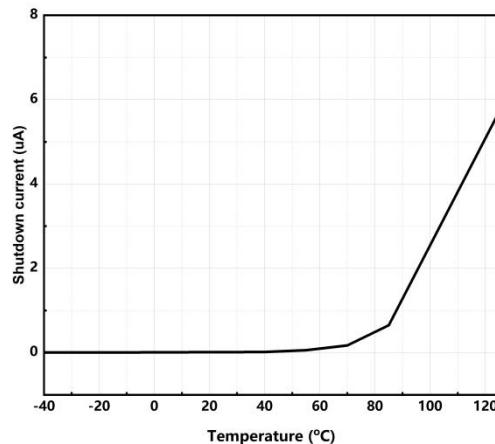
$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$  to  $500 \text{ mA}$

Figure 14. Load transient response



$V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $EN = 0 \text{ V}$

Figure 15. Shutdown current vs. Input voltage



$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{OUT} = 1 \mu\text{F}$ ,  $EN = 0 \text{ V}$

Figure 16. Shutdown current vs. Temperature

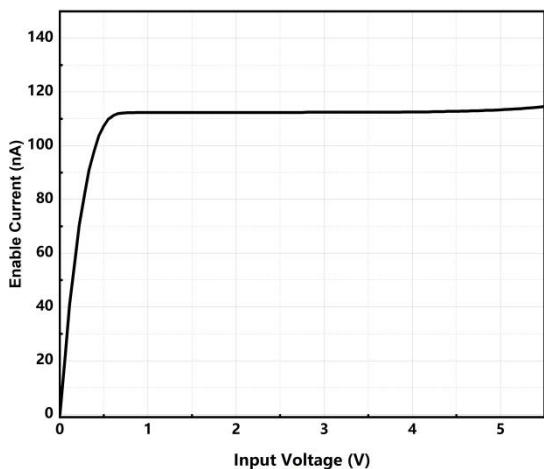
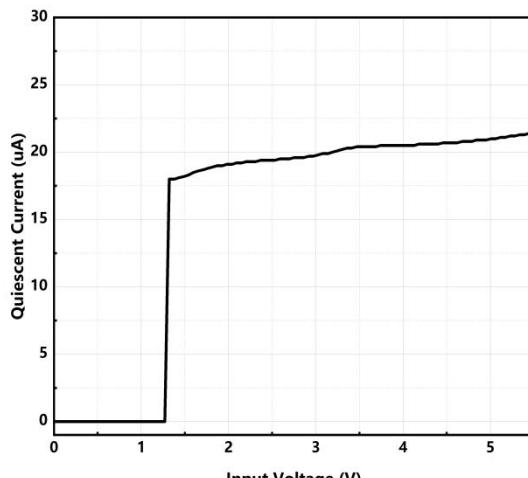
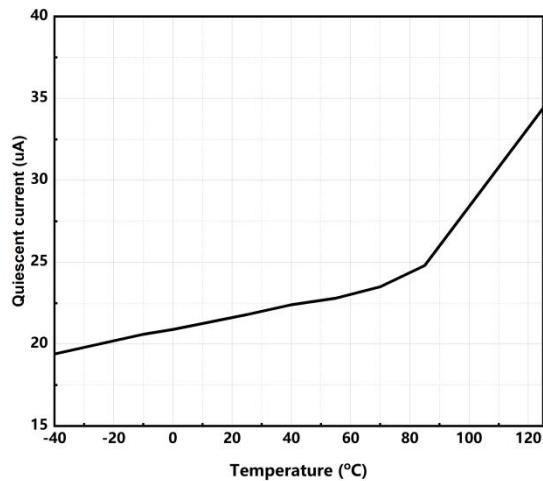


Figure 17. Enable current vs. Input voltage



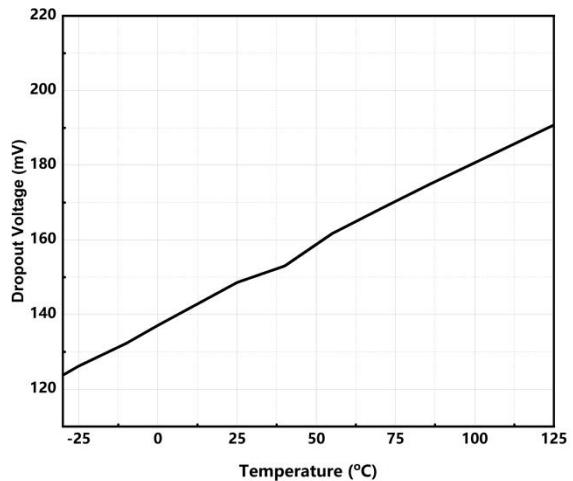
$V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $EN = 1 \text{ V}$

Figure 18. Quiescent current vs. Input voltage



$V_{IN} = 4.3 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $EN = 1 \text{ V}$

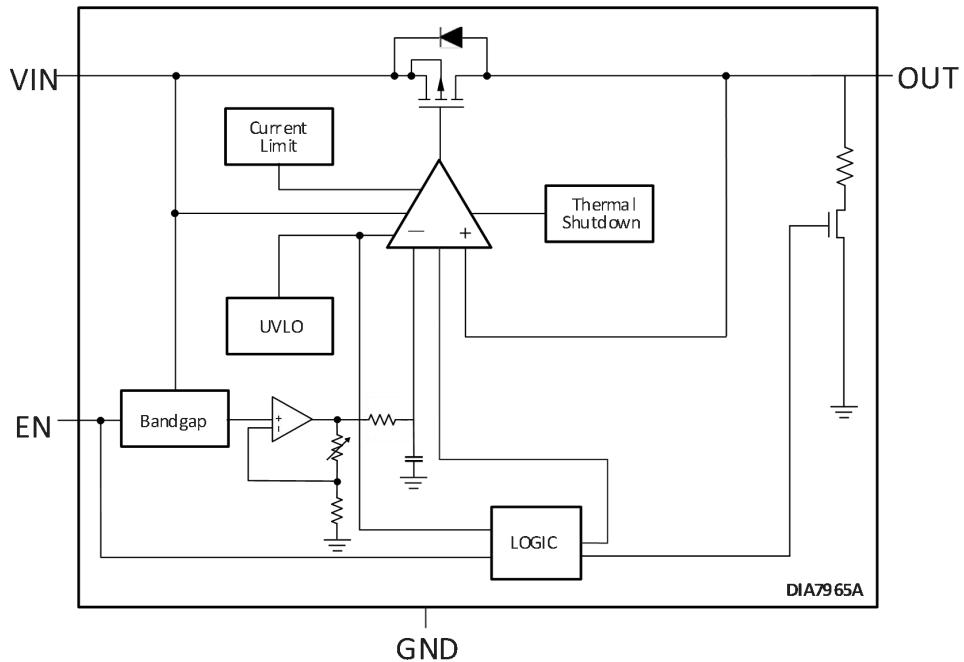
Figure 19. Quiescent current vs. Temperature



$V_{OUT} = 3.3 \text{ V}$ ,  $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $EN = 1 \text{ V}$

Figure 20. Dropout voltage vs. Temperature

## 8. Block Diagram



## 9. Function Description

The DIA7965 series of LDO linear regulators are ultra-high PSRR and low noise devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provide overall  $\pm 2\%$  accuracy. Low output noise, very high PSRR, and low dropout voltage make this device ideal for most battery-operated handheld equipment. The DIA7965 is fully protected in case of current overload, output short circuit, and overheating.

### 9.1. Input capacitor selection ( $C_{IN}$ )

The DIA7965 is specifically designed to work with a standard ceramic input capacitor. An Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used because of its minimal variation in values and equivalent series resistance (ESR) over temperature. The value of the input capacitor should be 1  $\mu F$  or larger to ensure the optimum dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

### 9.2. Output capacitor selection ( $C_{OUT}$ )

The DIA7965 requires an output capacitance, and the value of the input capacitor should be 1  $\mu F$  or larger for stability. Use X5R and X7R ceramic capacitors because of its minimal variation in value and equivalent series resistance (ESR) over temperature. Select a minimum effective capacitance of 0.7  $\mu F$  for  $C_{OUT}$ , considering capacitance changes with temperature, DC bias and package size. A capacitance of 0.7  $\mu F$  or higher can satisfy the requirement of all levels of  $V_{IN}$ ,  $V_{OUT}$ , and load.

Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperatures.

### 9.3. Enable operation

The DIA7965 uses the EN pin to enable or disable its device and discharge function (just for DIA7965A). If the EN pin voltage is pulled below 0.4 V, the device is guaranteed to be disabled. The active discharge transistor in the devices with the active discharge feature is activated and the output voltage  $V_{OUT}$  is pulled to GND through an internal circuitry with an effective resistance of about 100  $\Omega$ .

If the EN pin voltage is higher than 1.0 V the device is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is available at the output pin. In case of the enable function is not required, the EN pin should be connected directly to the input pin.

## 9.4. Output current limit

The DIA7965 internal current limit helps to protect the regulator during fault conditions. Output current is internally limited within the IC to a typical 700 mA. During the current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and  $V_{OUT} = I_{CL} \times R_{LOAD}$ . The PMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{CL}$  until the thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between the current limit and thermal shutdown.

## 9.5. Short circuits protection

The DIA7965 has integrated internally the function of short circuit protection for the device. When the output is shorted, the short circuit protection will limit the output current to a typical 200 mA, which is called short circuit limit ( $I_{SC}$ ). When a short circuit occurs, the PMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{SC}$  until the thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit.

## 9.6. Thermal shutdown

When the chip temperature exceeds the thermal shutdown point ( $T_{SD} = 160^{\circ}\text{C}$  typical), the device goes to the disabled state and the output voltage is not delivered until the die temperature decreases to  $135^{\circ}\text{C}$ . The thermal shutdown feature protects from a catastrophic device failure at accidental overheating. Using this protection in place of proper heat sinking is not recommended.

## 9.7. Dropout voltage

The DIA7965 uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(on)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device behaves as a resistor in dropout.

## 9.8. Power dissipation and heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the DIA7965 device can handle is given by:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (1)$$

The power dissipated by the DIA7965 device for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \times I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad (2)$$

## 9.9. Power supply rejection ratio

The DIA7965 features a very high Power Supply Rejection ratio to meet the requirements of RF and analog circuits. If desired the PSRR at higher frequencies in the range 100 kHz ~ 1 MHz can be tuned by the selection of  $C_{OUT}$  capacitor and proper PCB layout.

## 9.10. Turn-on time

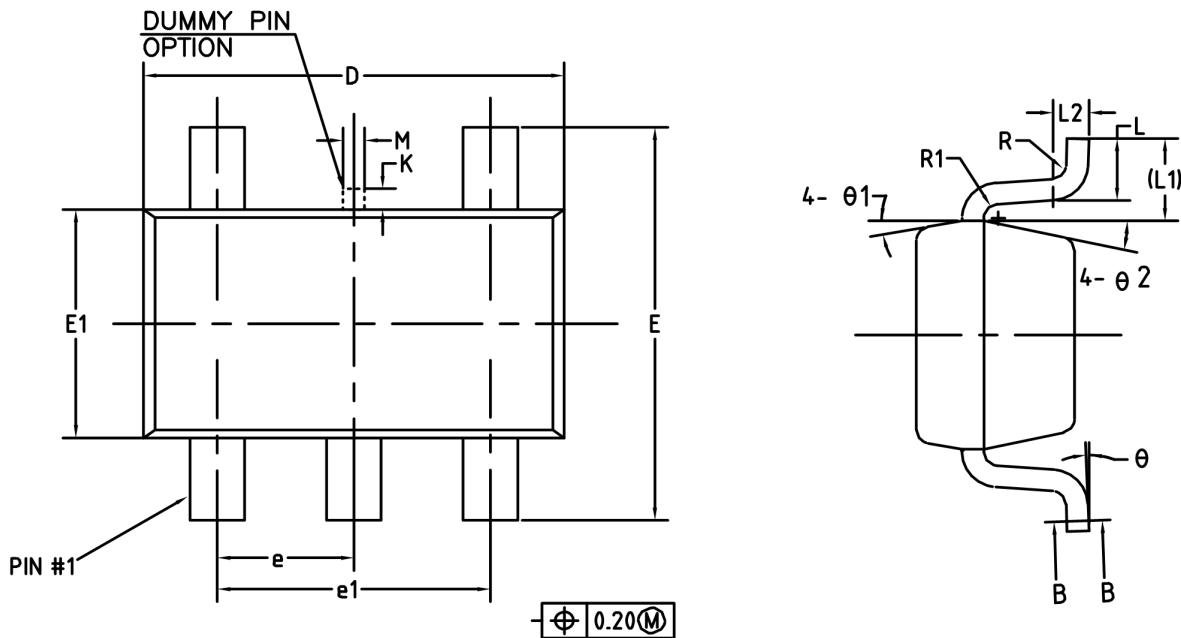
The turn-on time is defined as the time period from EN activation to the point in which  $V_{OUT}$  will reach 90% of its nominal value. The time is dependent on various application conditions such as  $V_{OUT(NOM)}$ ,  $C_{OUT}$ ,  $T_A$ .

# 10. Layout Guidelines

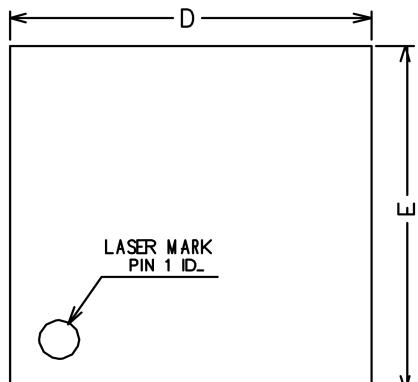
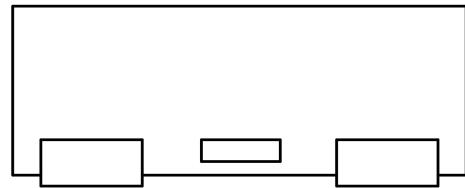
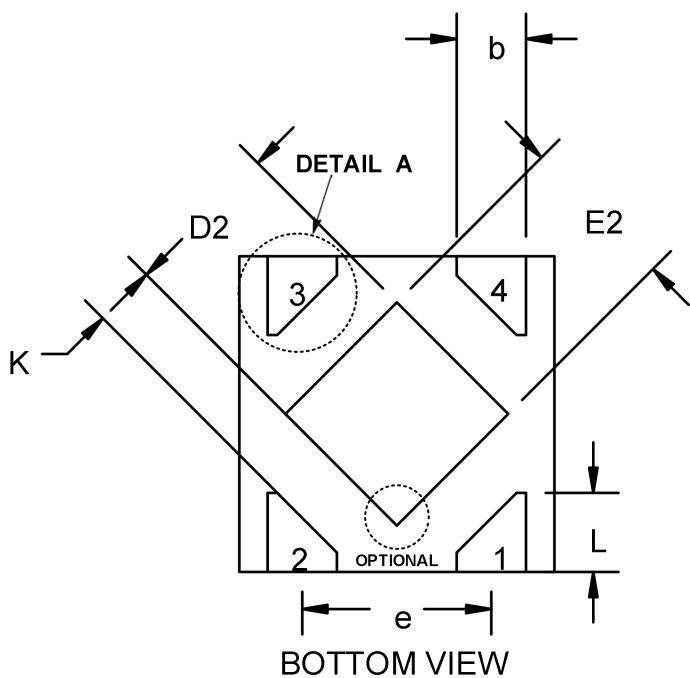
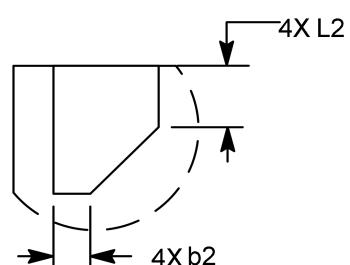
An optimal layout can greatly improve transient performance, PSRR, and noise.  $C_{IN}$  and  $C_{OUT}$  capacitors should be placed near device pins and PCB traces should be widely spaced for excellent performance. Place ground return connections to the input and output capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. For better power dissipation and lower device temperatures, tie the exposed pad to the GND pin.

## 11. Physical Dimensions

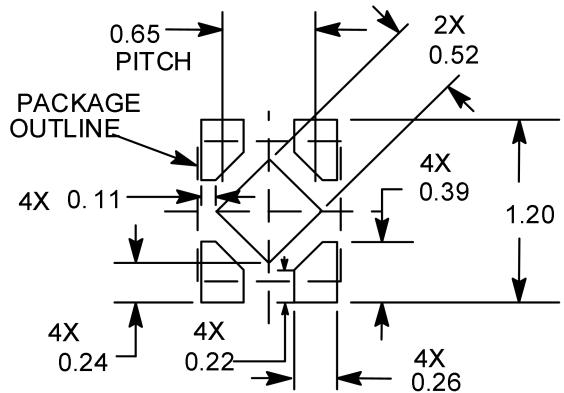
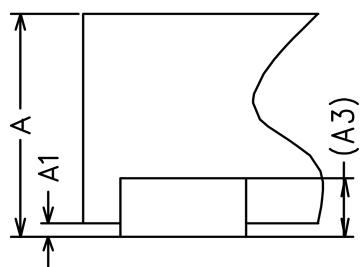
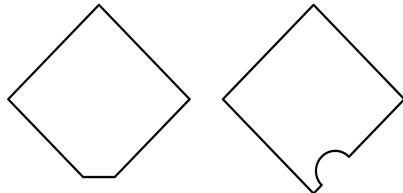
### 11.1. SOT23-5



Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
K	0	-	0.25
L	0.30	0.40	0.60
L1	0.59 REF		
L2	0.25 BSC		
M	0.10	0.15	0.25
R	0.05	-	0.20
R1	0.05	-	0.20
$\theta$	$0^\circ$	-	$8^\circ$
$\theta 1$	$8^\circ$	$10^\circ$	$12^\circ$
$\theta 2$	$10^\circ$	$12^\circ$	$14^\circ$

**11.2. DFN1\*1-4**

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**DETAIL A**

Two options:


**RECOMMENDED LAND PATTERN (Unit: mm)**

<b>Common Dimensions</b> <b>(Units of measure = Millimeter)</b>			
<b>Symbol</b>	<b>Min</b>	<b>Nom</b>	<b>Max</b>
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3	0.10 REF		
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	0.60	0.65	0.70
K	0.15	-	-
L2	0.07	0.12	0.17
b2	0.02	-	0.12

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