

DIO7976

500 mA, Ultra-Low Noise and High PSRR LDO for RF and Analog Circuits

Features

- Operating input voltage range: 1.7 V to 6.0 V
- Operating output voltage range:
 - Fixed option: 0.65 V to 5.0 V
 - Adjustable option: 0.55 V to 5.5 V
- Output current: 500 mA
- Ultra-high PSRR: 64 dB at 1 kHz (typ)
- Ultra-low noise: 40 μV_{RMS}
- Output voltage accuracy: $\pm 1\%$ at 25°C
- Ultra-low quiescent current: 27 μA (typ)
- Shutdown current: 0.1 μA (typ)
- Low dropout at 3.3 V: 150 mV at 500 mA
- Active output discharge: DIO7976A
- Non-active output discharge: DIO7976B
- Power-good output options:
 - Open-drain: DIO7976AO and DIO7976BO
 - Push-pull: DIO7976AP and DIO7976BP
- Stable with a 1 μF small case size ceramic capacitors
- Small packages: DFN2*2-6, DFN3*3-8, and SOT23-5, DFN1.2*1.2-6 packages

Descriptions

The DIO7976 is a 500 mA, ultra-high PSRR, ultra-low noise, high-accuracy, low-dropout CMOS linear regulator with high ripple rejection. Designed to meet the requirements of RF and analog circuits, this device consumes low quiescent current and provides fast line and load transient performance. The DIO7976 is a flexible device by supporting an input voltage range from 1.7 V to 6.0 V. This device has a fixed output voltage option of 0.65 V to 5.0 V and an externally adjustable output range of 0.55 V to 5.5 V, making the device flexible for post-regulation.

The DIO7976 is designed to work with a 1 μF input and a 1 μF output ceramic capacitor, allowing for a small overall solution size. A precision band-gap and error amplifier provide a high-accuracy of $\pm 1\%$ (max) at 25°C. It is available in DFN2*2-6, DFN3*3-8, SOT23-5 and DFN1.2*1.2-6 packages.

Applications

- Battery powered equipment
- Wireless LAN devices
- Smartphones, tablets
- Cameras, DVRs, STB and camcorders



DIO7976

500 mA, Ultra-Low Noise and High PSRR LDO for RF and Analog Circuits

Ordering Information

Ordering Part No.	Top Marking	MSL	Description	RoHS	T _A	Package	
DIO7976AOaaCD6	GF5XO	3	Active Discharge	Green	-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976APaaCD6	GF5XP	3		Green	-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976AOaaCD8	GF5XO	3		Green	-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976APaaCD8	GF5XP	3		Green	-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976AaaST5	YWA5X	3		Green	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO7976AOADJCD6	GF5XO	3		Green	-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976APADJCD6	GF5XP	3		Green	-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976AOADJCD8	GF5XO	3		Green	-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976APADJCD8	GF5XP	3		Green	-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976AADJST5	YWA5X	3		Green	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO7976AADJPN6	AXYW	1		Green	-40 to 125°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO7976BOaaCD6	GF7XO	3		Non-Active Discharge	Green	-40 to 125°C	DFN2*2-6
DIO7976BPaaCD6	GF7XP	3	Green		-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976BOaaCD8	GF7XO	3	Green		-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976BPaaCD8	GF7XP	3	Green		-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976BaaST5	YWA7X	3	Green		-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO7976BOADJCD6	GF7XO	3	Green		-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976BPADJCD6	GF7XP	3	Green		-40 to 125°C	DFN2*2-6	Tape & Reel, 3000
DIO7976BOADJCD8	GF7XO	3	Green		-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976BPADJCD8	GF7XP	3	Green		-40 to 125°C	DFN3*3-8	Tape & Reel, 5000
DIO7976BADJST5	YWA7X	3	Green		-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO7976BADJPN6	BXYW	1	Green		-40 to 125°C	DFN1.2*1.2-6	Tape & Reel, 5000

Output Voltage Options

Option Code "aa"	08	10	12	15	25	28	30	33
Voltage	0.8 V	1.0 V	1.2 V	1.5 V	2.5 V	2.8 V	3 V	3.3 V

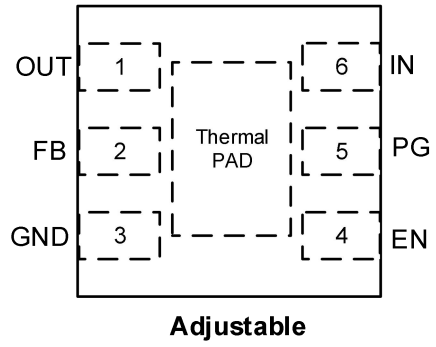
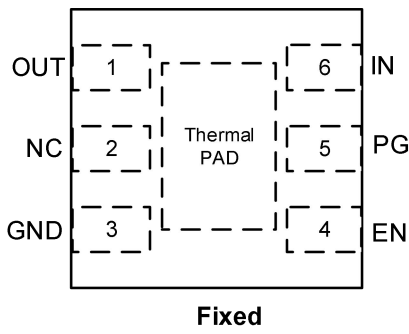
Marking Definition: GF5XO / GF5XP / YWA5X / GF7XO / GF7XP / YWA7X / AXYW / BXYW

GF5XO	GF: Product code; 5: Product code; X: Voltage code; O: Open-drain version.
GF5XP	GF: Product code; 5: Product code; X: Voltage code; P: Push-pull version.
YWA5X	Y: Year code; W: Week code; A: Product code; 5: Product code; X: Voltage code.
GF7XO	GF: Product code; 7: Product code; X: Voltage code; O: Open-drain version.
GF7XP	GF: Product code; 7: Product code; X: Voltage code; P: Push-pull version.
YWA7X	Y: Year code; W: Week code; A: Product code; 7: Product code; X: Voltage code.
AXYW	A: Product code; X: Voltage code; Y: Year code; W: Week code.
BXYW	B: Product code; X: Voltage code; Y: Year code; W: Week code.

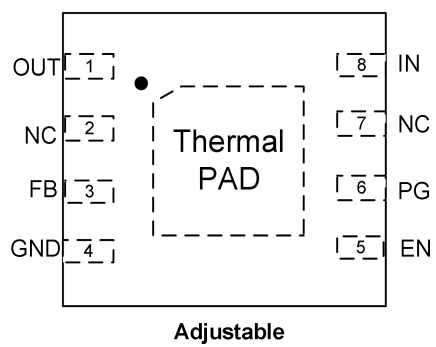
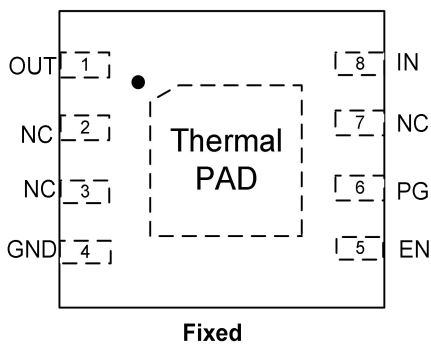
Voltage Code

Option Code "X"	C	D	F	G	J	K	L	M	Q
Voltage	0.8 V	1.0 V	1.2 V	1.5 V	2.5 V	2.8 V	3 V	3.3 V	ADJ

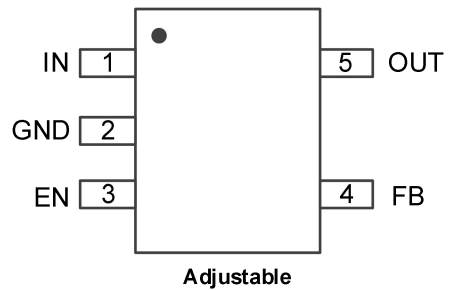
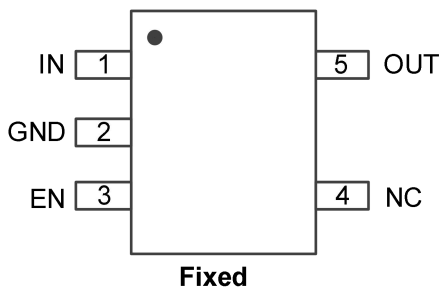
Pin Assignments



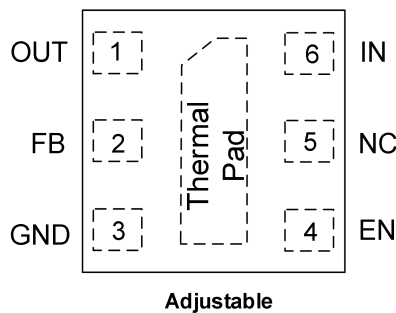
DFN2*2-6 (Top view)



DFN3*3-8 (Top view)



SOT23-5 (Top view)



DFN1.2*1.2-6 (Top view)

Figure 1. Pin assignment (Top view)

Pin Definitions

Pin Name	Description
EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
FB	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	Ground pin.
IN	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table. Place the input capacitor as close to the output of the device as possible.
NC	No internal connection. Ground this pin for better thermal performance.
OUT	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; Place the output capacitor as close to the output of the device as possible.
PG	Power-good output. Available in open-drain and push-pull topologies. A pull-up resistor is only required for the open-drain type. For the open-drain version (DIO7976AO and DIO7976BO), if the power-good functionality is not being used, ground this pin or leave floating. For the push-pull version (DIO7976AP and DIO7976BP), if the power-good functionality is not being used, leave this pin floating.
Thermal Pad	The thermal pad is left floating. Connect to the GND plane for improved thermal performance.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage	-0.3 to 6.6	V
V_{OUT}	Output voltage	-0.3 to $V_{IN} + 0.3$ ⁽¹⁾	V
V_{EN}	Enable voltage	-0.3 to 6.6	V
V_{FB}	Feedback voltage	-0.3 to 2	V
I_{OUT}	Output current	Internally limited	
I_{PG}	Power-good current	-10 to 10	mA
T_J	Operating junction temperature	-40 to 125	°C
T_{STG}	Storage temperature	-65 to 150	

Note:

(1) The absolute maximum rating is $V_{IN} + 0.3$ V or 6.0 V, whichever is smaller.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter		Rating	Unit
V_{IN}	Input voltage		1.7 to 6	V
V_{OUT}	Output voltage	Adjustable only	0.55 to 5.5	V
		Fixed only	0.65 to 5	
I_{OUT}	Output current		0 to 500	mA
C_{IN}	Input capacitor		≥ 1	μF
C_{OUT}	Output capacitor ⁽¹⁾		1 to 22	μF
C_{FF}	Feed-forward capacitor		10	nF
V_{EN}	Enable voltage		0 to 6	V
T_J	Junction operating temperature		-40 to 125	$^{\circ}\text{C}$
ESD	Human-body model		± 4000	V
	Charged-device model		± 2000	

Note:

(1) Minimum derated capacitance of 0.47 μF is required for stability.

Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOT23-5	115	$^{\circ}\text{C}/\text{W}$
		DFN3*3-8	48	
		DFN2*2-6	102	
$R_{\theta JC}$	Junction-to-case thermal resistance	SOT23-5	32	$^{\circ}\text{C}/\text{W}$
		DFN2*2-6	48	

Electrical Characteristics

At operating temperature range ($T_A = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(NOM)} + V_{DO}$ or 1.7 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted; all typical values are at $T_A = 25^{\circ}\text{C}$.

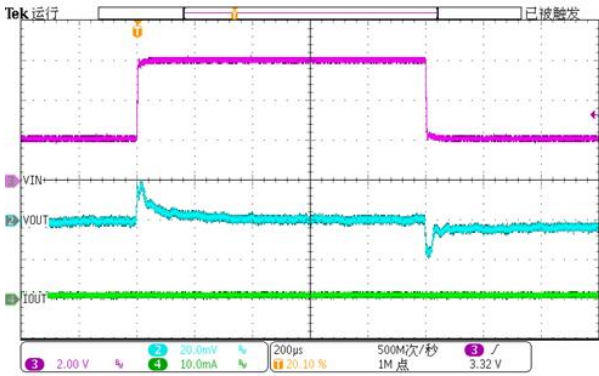
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
V_{FB}	Feedback voltage	Adjustable only	0.545	0.55	0.555	V	
V_{IN}	Operating input voltage		1.7		6	V	
	Output voltage accuracy ⁽¹⁾	$I_{OUT} = 1\text{ mA}$, $T_A = 25^{\circ}\text{C}$	-1		1	%	
Line _{Reg}	Line regulation	$V_{OUT(NOM)} + V_{DO} \leq V_{IN}^{(2)} \leq 6.0\text{ V}$, $T_A = 25^{\circ}\text{C}$		0.1	0.3	%/V	
Load _{Reg}	Load regulation	$0.1\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$, $V_{IN} \geq 2.0\text{ V}$		0.04		V/A	
V_{DO}	Dropout voltage	$I_{OUT} = 500\text{ mA}$, $V_{OUT} = 0.95 \times$ $V_{OUT(NOM)}$	$V_{OUT} = 1\text{ V}$		830		mV
			$V_{OUT} = 1.2\text{ V}$		650		
			$V_{OUT} = 1.5\text{ V}$		400		
			$V_{OUT} = 1.8\text{ V}$		270		
			$V_{OUT} = 2.5\text{ V}$		185		
			$V_{OUT} = 3.3\text{ V}$		150		
			$V_{OUT} = 5.5\text{ V}$		115		
I_{CL}	Output current limit	$V_{OUT(NOM)} < 1.0\text{ V}$, $T_A = 25^{\circ}\text{C}$ $V_{OUT} = V_{OUT(NOM)} - 0.2\text{ V}$, $V_{IN} = 2.0\text{ V}$	515	720	1000	mA	
		$V_{OUT(NOM)} \geq 1.0\text{ V}$, $V_{OUT} = V_{OUT(NOM)} \times 0.85$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$, $T_A = 25^{\circ}\text{C}$					
I_{SC}	Short circuit current	$V_{OUT} = 0\text{ V}$	$V_{OUT(NOM)} < 1.0\text{ V}$, $V_{IN} = 2.0\text{ V}$, $T_A = 25^{\circ}\text{C}$	200	300	400	mA
			$V_{OUT(NOM)} \geq 1.0\text{ V}$, $T_A = 25^{\circ}\text{C}$				
			$V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$				
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$, $T_A = 25^{\circ}\text{C}$		27	45	μA	
I_{DIS}	Shutdown current	$V_{EN} \leq 0.3\text{ V}$, $1.7\text{ V} \leq V_{IN} \leq 6.0\text{ V}$, $T_A = 25^{\circ}\text{C}$		0.1	1	μA	
I_{FB}	Feedback pin current	Adjustable only, $T_A = 25^{\circ}\text{C}$		0.01	0.1	μA	
V_{ENH}	EN pin threshold voltage	EN Input voltage "H", $T_A = 25^{\circ}\text{C}$	1			V	
V_{ENL}		EN Input voltage "L", $T_A = 25^{\circ}\text{C}$			0.3	V	
I_{EN}	EN pull down current	$V_{IN} = V_{EN} = 6.0\text{ V}$		10		nA	
t_{STR}	Startup time	From EN low-to-high transition to $V_{OUT} = V_{OUT(NOM)} \times 0.95$, $T_A = 25^{\circ}\text{C}$	200	450	800	μs	
PSRR	Power supply rejection ratio	$V_{OUT} = 0.55\text{ V}$, $V_{IN} = 2.0\text{ V}$, $I_{OUT} = 10\text{ mA}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$	$f = 1\text{ kHz}$		64		dB
			$f = 100\text{ kHz}$		50		
			$f = 1\text{ MHz}$		75		
V_N	Output voltage noise	$V_{OUT} = 0.55\text{ V}$, $V_{IN} = 2.0\text{ V}$		40		μV_{RMS}	

V _{UVLO}	Undervoltage lockout	V _{IN} falling, T _A = 25 °C	1.17	1.27		V
		V _{IN} rising, T _A = 25 °C		1.32	1.55	
V _{UVLO,HYST}	Undervoltage lockout hysteresis	V _{IN} hysteresis		50		mV
T _{SDH}	Thermal shutdown threshold	Temperature rising		165		°C
T _{SDL}		Temperature falling		150		°C
R _{PULLDOWN}	Pulldown resistance	V _{IN} = 6.0 V		100		Ω
PG _H TH	PG high threshold	V _{OUT} increasing, T _A = 25°C		92		%V _{OUT}
PG _L TH	PG low threshold	V _{OUT} decreasing, T _A = 25°C		90		%V _{OUT}
PG _H YST	PG hysteresis			2		%V _{OUT}
V _{OL(PG)}	PG pin low-level output voltage	V _{IN} ≥ 1.7 V, I _{SINK} = 1.0 mA, T _A = 25°C			400	mV
		V _{IN} ≥ 2.75 V, I _{SINK} = 2.0 mA, T _A = 25°C				
V _{OH(PG)}	PG pin high-level output voltage ⁽³⁾	V _{OUT} ≥ 1.0 V, I _{SOURCE} = 0.04 mA, T _A = 25°C	0.8 x	V _{OUT}		V
		V _{OUT} ≥ 1.4 V, I _{SOURCE} = 0.2 mA, T _A = 25°C				
		V _{OUT} ≥ 2.5 V, I _{SOURCE} = 0.5 mA, T _A = 25°C				
		V _{OUT} ≥ 4.5 V, I _{SOURCE} = 1.0 mA, T _A = 25°C				
I _{kg(PG)}	PG pin leakage current ⁽⁴⁾	V _{OUT} > PG _H TH, V _{PG} = 6.0 V, T _A = 25°C		7	50	nA
t _{PGDH}	PG delay time rising	Time from 92% V _{OUT} to 20% of PG ⁽⁵⁾		165		μs
t _{PGDL}	PG delay time falling	Time from 90% V _{OUT} to 80% of PG ⁽⁵⁾		12		

Note:

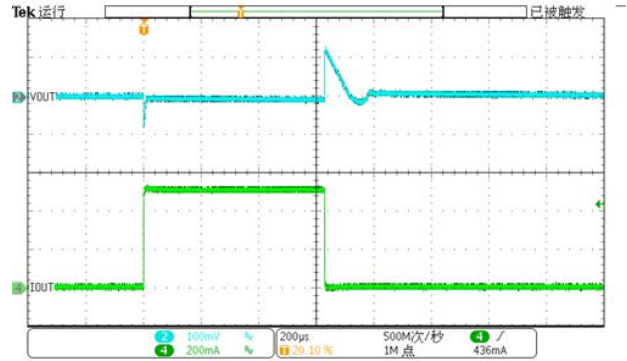
- (1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
- (2) V_{IN} = 1.7 V for V_{OUT(NOM)} + V_{DO} < 1.7 V.
- (3) Push-pull version only. The push-pull option is supported only for V_{OUT} ≥ 1.0 V.
- (4) Open-drain version only.
- (5) Output overdrive = 10%.
- (6) Specifications subject to change without notice.

Typical Characteristics



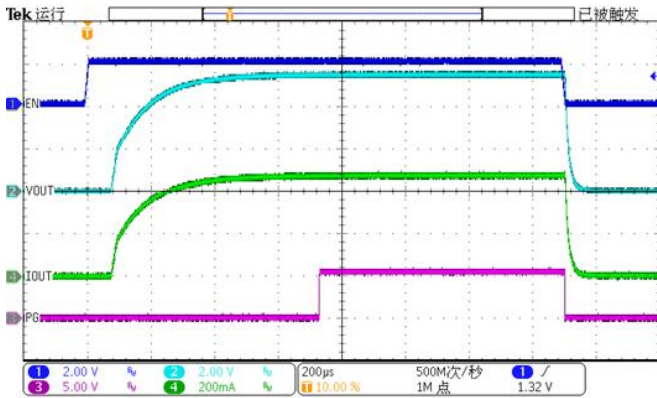
$V_{OUT} = 0.55\text{ V}$, $V_{IN} = 2\text{ V} \leftrightarrow 6\text{ V}$ at $1\text{ V}/\mu\text{s}$, $I_{OUT} = 1\text{ mA}$

Figure 2. Line transient



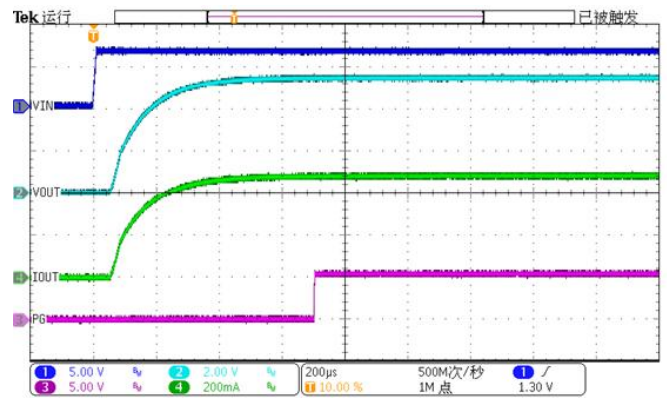
$V_{IN} = 6\text{ V}$, $V_{OUT} = 5.5\text{ V}$, $1\text{ mA} \leftrightarrow 500\text{ mA}$ at $1\text{ }\mu\text{s}$

Figure 3. Load transient



$V_{IN} = 6\text{ V}$, $V_{OUT} = 5.5\text{ V}$, $I_{OUT} = 500\text{ mA}$

Figure 4. Star up with EN



$V_{IN} = 6\text{ V}$, $V_{OUT} = 5.5\text{ V}$, $I_{OUT} = 500\text{ mA}$

Figure 5. Power up with V_{IN}

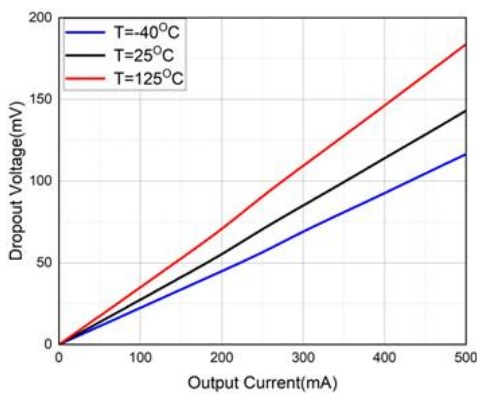


Figure 6. Dropout voltage vs. I_{OUT} at $V_{OUT} = 3.3\text{ V}$

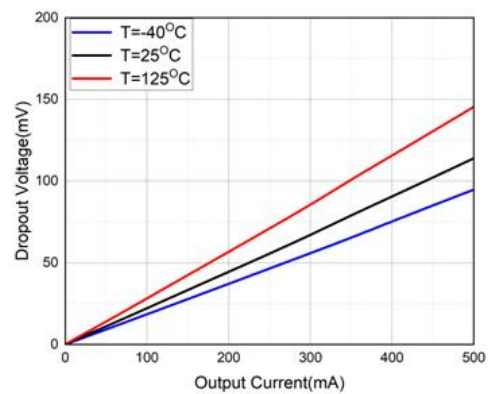
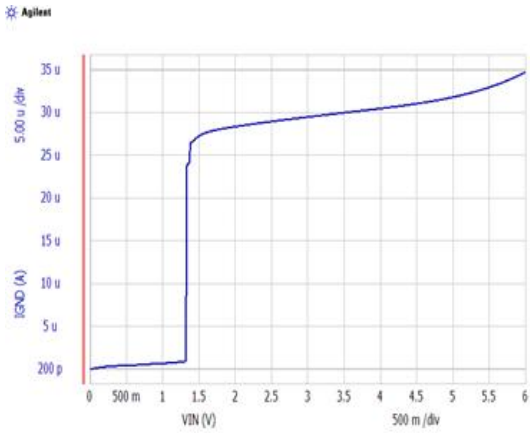
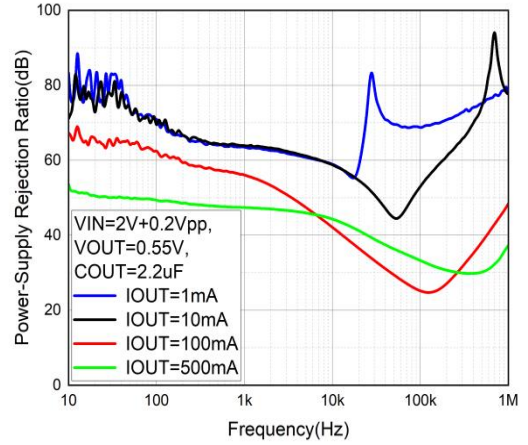


Figure 7. Dropout voltage vs. I_{OUT} at $V_{OUT} = 5.5\text{ V}$



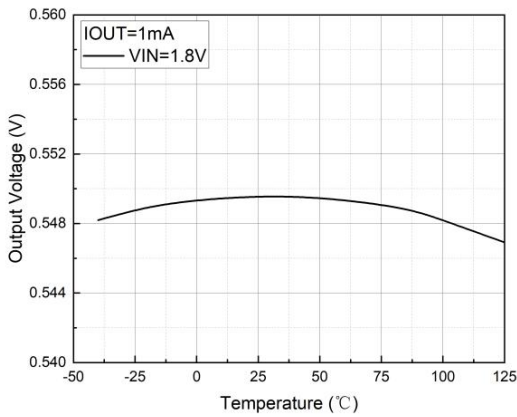
$V_{OUT} = 0.55\text{ V}$, $I_{OUT} = 0\text{ mA}$

Figure 8. I_{GND} vs. V_{IN}



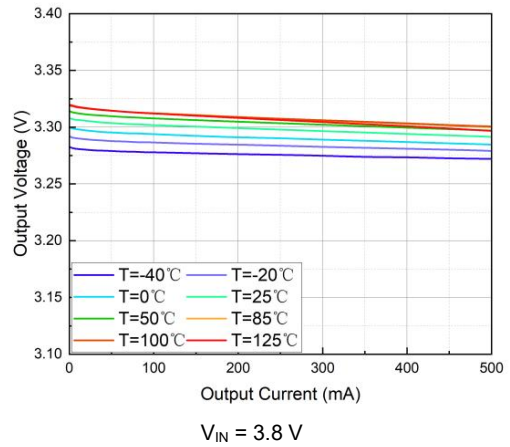
$V_{IN} = 2\text{ V}$, $V_{OUT} = 0.55\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$

Figure 9. PSRR vs. Frequency and I_{OUT}



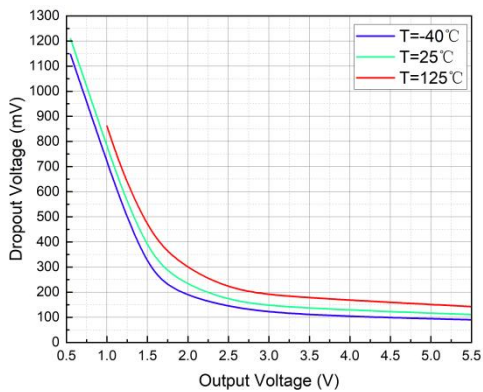
$V_{OUT} = 0.55\text{ V}$, $I_{OUT} = 1\text{ mA}$

Figure 10. Output voltage vs. Temperature



$V_{IN} = 3.8\text{ V}$

Figure 11. Output voltage vs. Output current



$I_{OUT} = 500\text{ mA}$

Figure 12. Dropout voltage vs. Output voltage

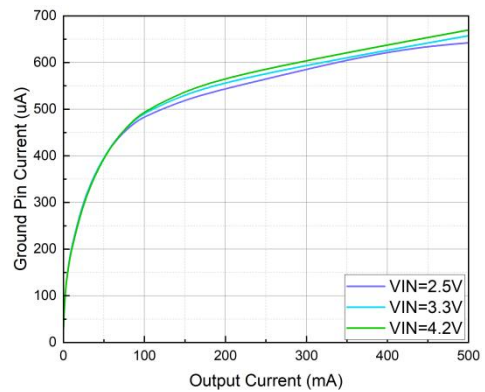


Figure 13. Ground pin current vs. Output current

Block Diagram

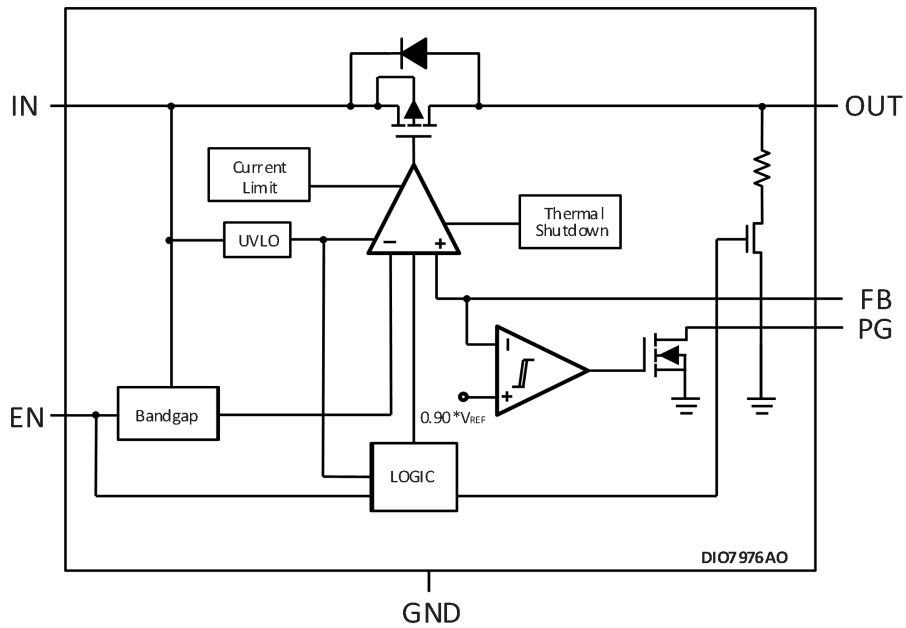


Figure 14. Adjustable version with open-drain power-good

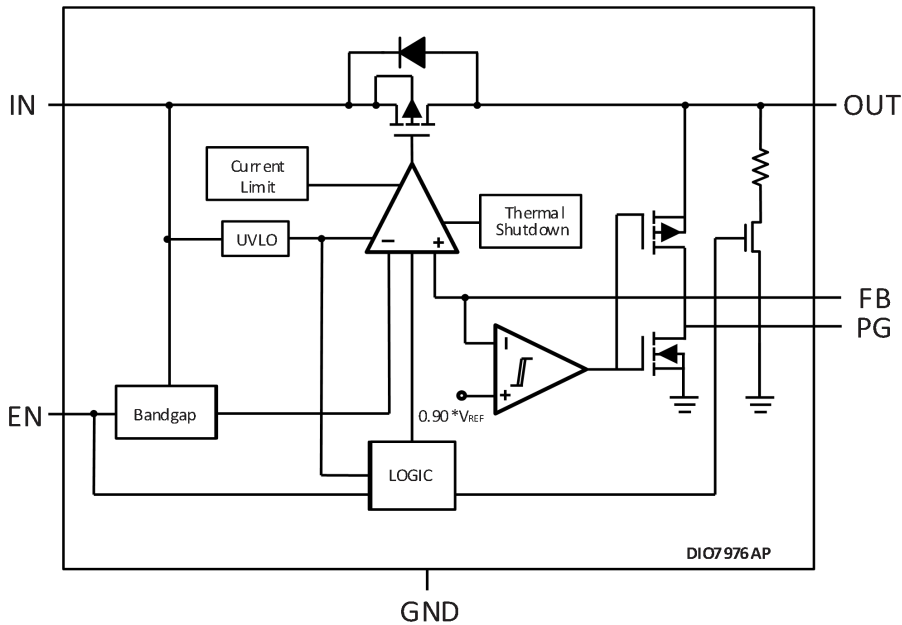


Figure 15. Adjustable version with push-pull power-good

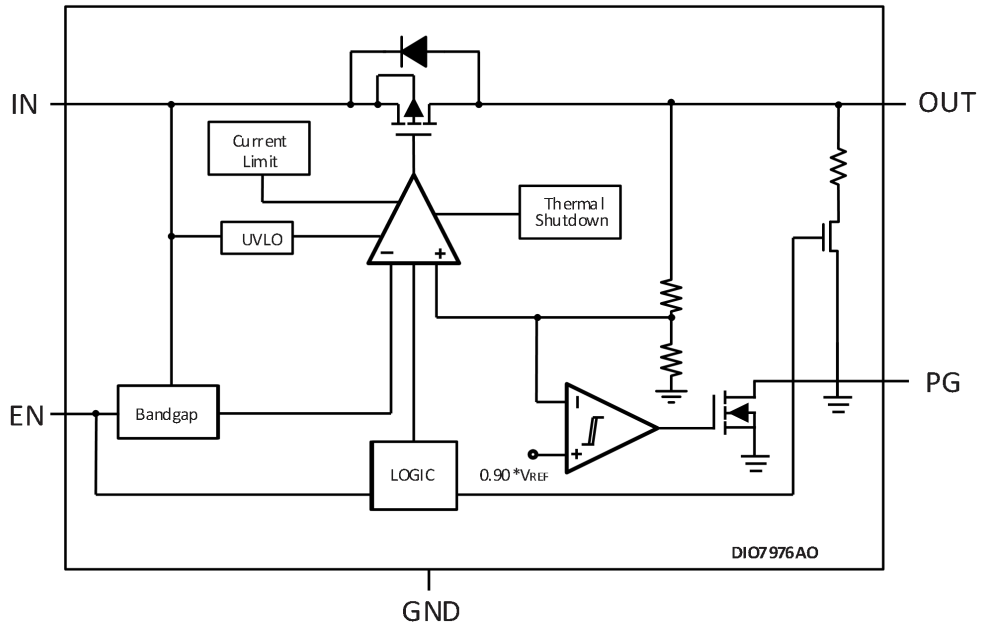


Figure 16. Fixed voltage version with open-drain power-good

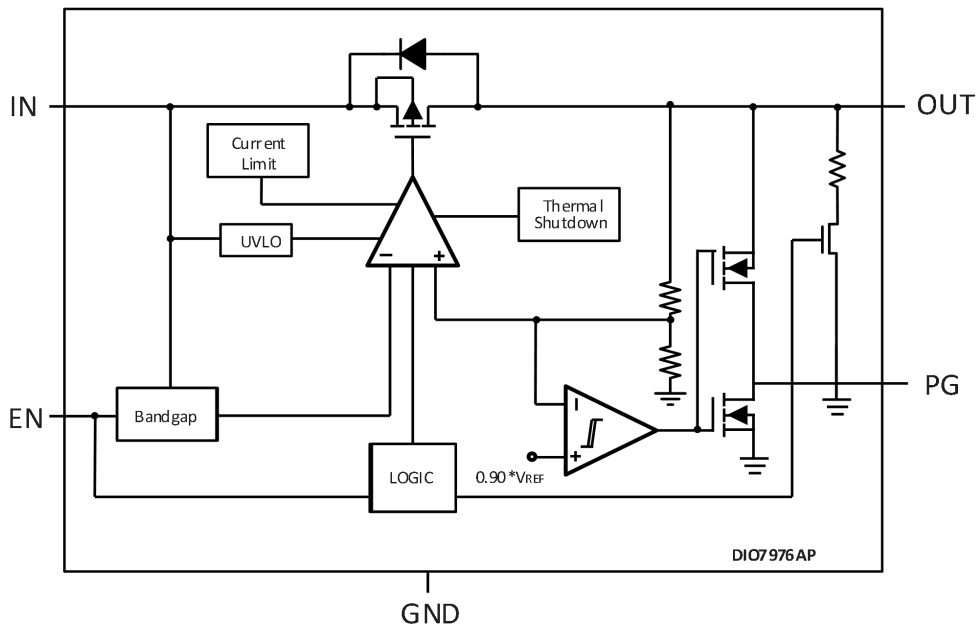


Figure 17. Fixed voltage version with push-pull power-good

Applications Information

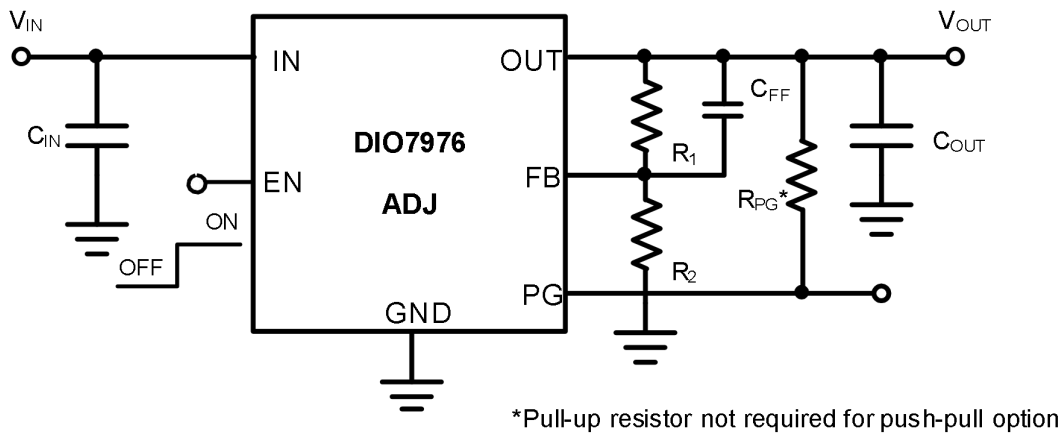


Figure 18. Typical application: adjustable voltage

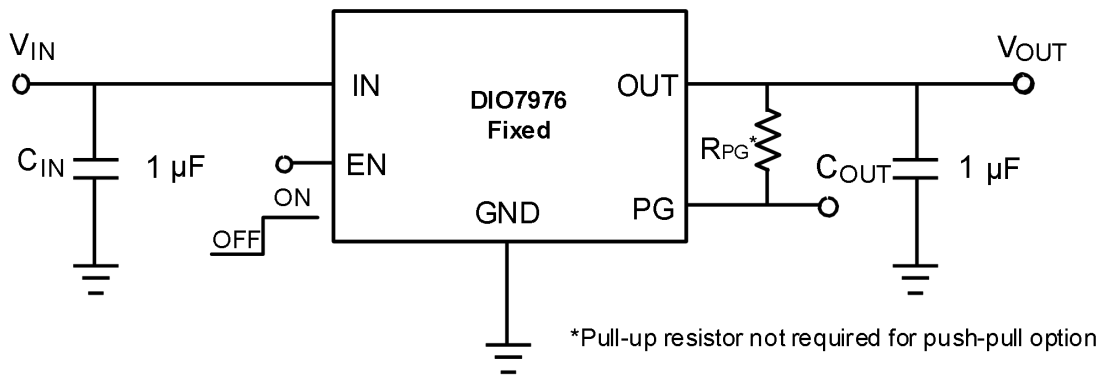


Figure 19. Typical application: fixed voltage

Overview

The DIO7976 is a low-dropout regulator (LDO) that consumes a low quiescent current and delivers an excellent line and load transient performance. These characteristics, combined with low noise and high PSRR with low dropout voltage, make this device ideal for different applications.

This regulator offers short-current limit, shutdown, and thermal protection. The operating junction temperature for this device is -40°C to 125°C .

Undervoltage lockout (UVLO)

The DIO7976 contains an undervoltage lockout (UVLO) circuit that ensures that the device is functional when the supply voltage is lower than the operational range of the internal circuitry, which disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). When V_{IN} is less than V_{UVLO} , the output is connected to the ground with a pulldown resistor ($R_{PULLDOWN}$). When the device enters UVLO, the PG output is pulled low.

Shutdown

The enable pin (EN) is active high. Forcing the EN pin to exceed $V_{EN(HI)}$ will enable the device forcing the EN pin to drop below $V_{EN(LO)}$ will turn off the device. Connect EN to IN when shutdown capability is not required. The PG output pin is pulled low when the device is disabled. The DIO7976 has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to the ground when the device is disabled. Output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor ($R_{PULLDOWN}$) decide the discharge time after disabling. The equation below calculates the time constant:

$$T = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \times C_{OUT} \quad (1)$$

Current limit

The device is protected during transient high-load current faults or shorting events by an internal current limit circuit. The current limit is a hybrid scheme that transitions from a current-limit scheme to a short-limit scheme at the voltage about 0.3 V. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). In a high-load current fault with the output voltage above 0.3 V, the current-limit scheme limits the output current to I_{CL} . When the voltage drops below 0.3 V, a short-current limit activates that scales back the current as the output voltage approaches GND.

When the device is within the current limit, the output voltage is not regulated. The device begins to heat up when a current limit event occurs, and if a thermal shutdown is triggered, the device turns off. When the device is in current-limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below 0.3 V, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. The internal thermal shutdown circuit turns the device back on after the device cools down. The device cycles between the current limit and thermal shutdown if the output current fault condition continues.

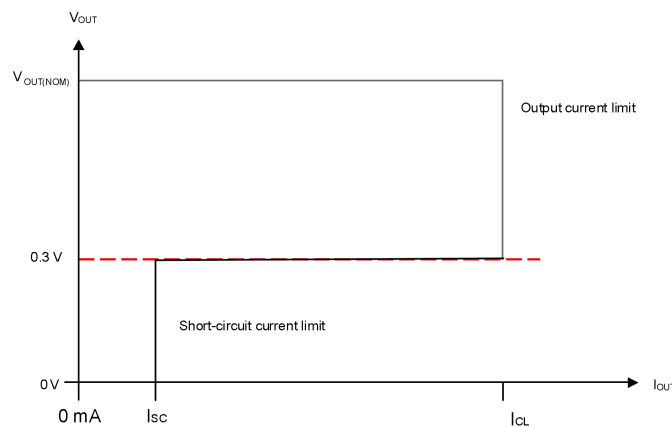


Figure 20. Current limit

Power-good function (PG)

To indicate the status of the output voltage, the power-good circuit monitors the voltage at the FB pin. If the output voltage is below PG_{LTH} (PG low threshold), the PG pin open-drain output activates and pulls the PG pin close to GND. If the output voltage is higher than PG_{HTh} (PG high threshold), then the PG pin will be high impedance.

A pull-up resistor is needed for the open-drain output. Any downstream device can receive power-good as a logic signal for sequencing through attaching a pull-up resistor to an external supply. Furthermore, the open-drain output may be linked to other open-drain outputs to implement AND logic. Check to see if the external pull-up supply voltage produces a valid logic signal for the receiving device. It is advised to use a pull-up resistor ranging

from 10 kΩ to 100 kΩ. While for push-pull PG option, the pull-up resistor is not needed. The push-pull PG option has a high logic signal correlating with the output voltage. The push-pull option is only valid for $V_{OUT} \geq 1\text{ V}$ and please do not link the push-pull output to other logic outputs.

If C_{FF} (feed-forward capacitor) is used, the time constant for the LDO start-up is increased while the time constant for PG output remains unchanged, which may leading to an invalid PG output. To avoid the situation, DIOO recommend to ensure the time constant of both LDO start-up and PG output match by adding a capacitor in parallel with the power-good pull-up resistor.

To make the PG valid, the device should operate above the minimum V_{IN} and PG is asserted, regardless of the output voltage state when V_{IN} is below V_{UVLO} minus $V_{UVLO, HYST}$. When V_{IN} falls below about 0.8 V, power-good device turns on and the power-good output pulls high because of no enough gate drive voltage to keep the open-drain. This effect can be minimized by connecting the PG pull-up resistor to the output voltage.

Thermal shutdown

The DIO7976 has a thermal shutdown protection feature that disables the device when the junction temperature rises to approximately 165°C. This feature helps to reduce the power dissipated by the device, allowing it to cool down. When the temperature falls to approximately 150°C, the output circuitry is re-enabled. However, depending on various factors like power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may turn on and off repeatedly. This cycling helps to limit regulator dissipation and protect the regulator from overheating damage. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the $(V_{IN} - V_{OUT})$ voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increasing the ambient temperature until the thermal protection is triggered, use worst-case loads and signal conditions.

The DIO7976 has a built-in protection circuit that guards against overload conditions. However, it doesn't mean to be triggered during regular operation. Running the device continuously into thermal shutdown can harm the device's reliability.

Device functional modes

The Device Functional Mode Comparison table shows the conditions that lead to the different modes of operation.

Table 1. Device functional modes

Operating Mode	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

Note:

(1) See the Electrical Characteristics table for parameter values.

Dropout operation

If all conditions are met for normal operation but the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. During dropout mode, the output voltage

tracks the input voltage and the transient performance of the device becomes significantly degraded and acts as a switch line or load transients in dropout can result in large output-voltage deviations.

When the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but not during startup, the pass transistor is driven into the ohmic or triode region. The output voltage can overshoot for a short period while the device pulls the pass transistor back into the linear region when the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$).

Disabled

Shutting down the output of the device will require forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage. The pass transistor is turned off internal circuits are shutdown, and the output voltage is actively discharged to the ground by an internal discharge circuit from the output to the ground, when the device is disabled.

Adjustable device feedback resistors

Figure 14 shows that the output voltage of the DIO7976 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

The adjustable version DIO7976 requires external feedback divider resistors to set the output voltage. The feedback divider resistors, R_1 and R_2 set the V_{OUT} , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1/R_2) \quad (2)$$

Setting the feedback divider current to 100 x the FB pin current listed in the Electrical Characteristics table can ignore the FB pin current error term in the V_{OUT} equation, which provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

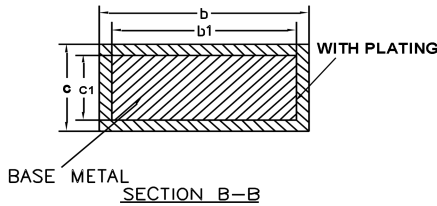
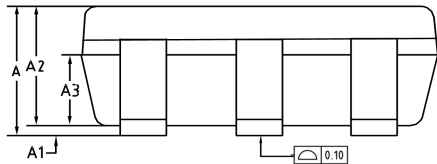
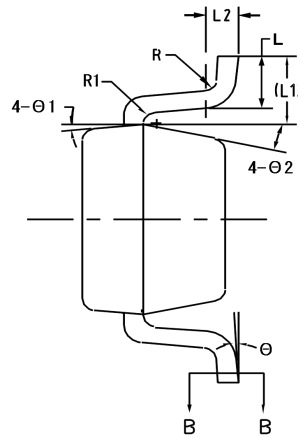
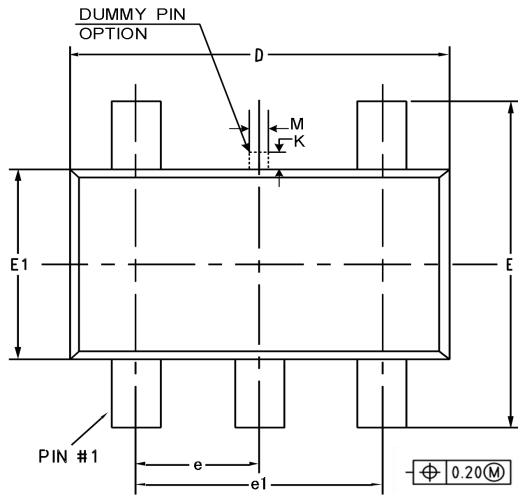
Table 2. Recommended resistors for DIO7976 (Adjustable version)

V_{OUT} (V)	R_1 (k Ω)	R_2 (k Ω)
0.55	0	Float
1	8.2	10
1.2	18.2	15.4
1.5	21	12.1
1.8	27.4	12
2.5	39	11
3.3	49.9	10
5.5	18	2

Dropout voltage

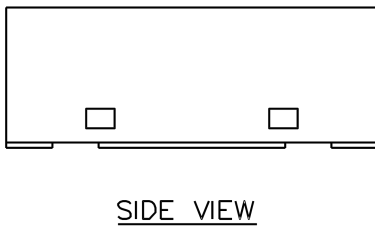
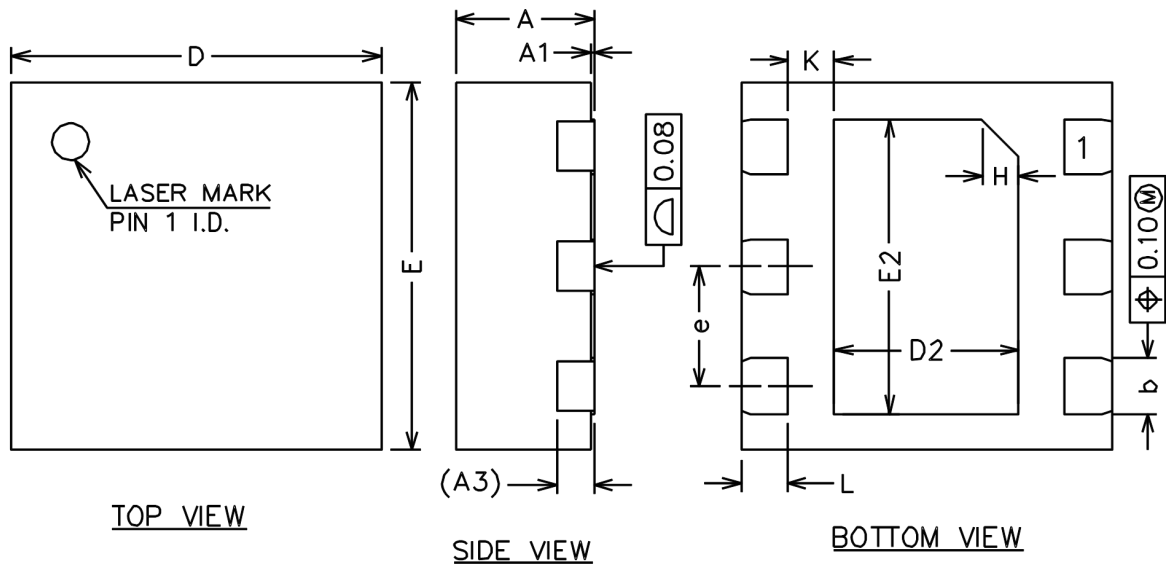
A PMOS pass transistor is used to achieve low dropout. The PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element when $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}). The PMOS device behaves like a resistor in dropout mode therefore V_{DO} scales approximately with the output current. PSRR and transient response degrade as $(V_{IN} - V_{OUT})$ approaches dropout operation with any linear regulator.

Physical Dimensions: SOT23-5



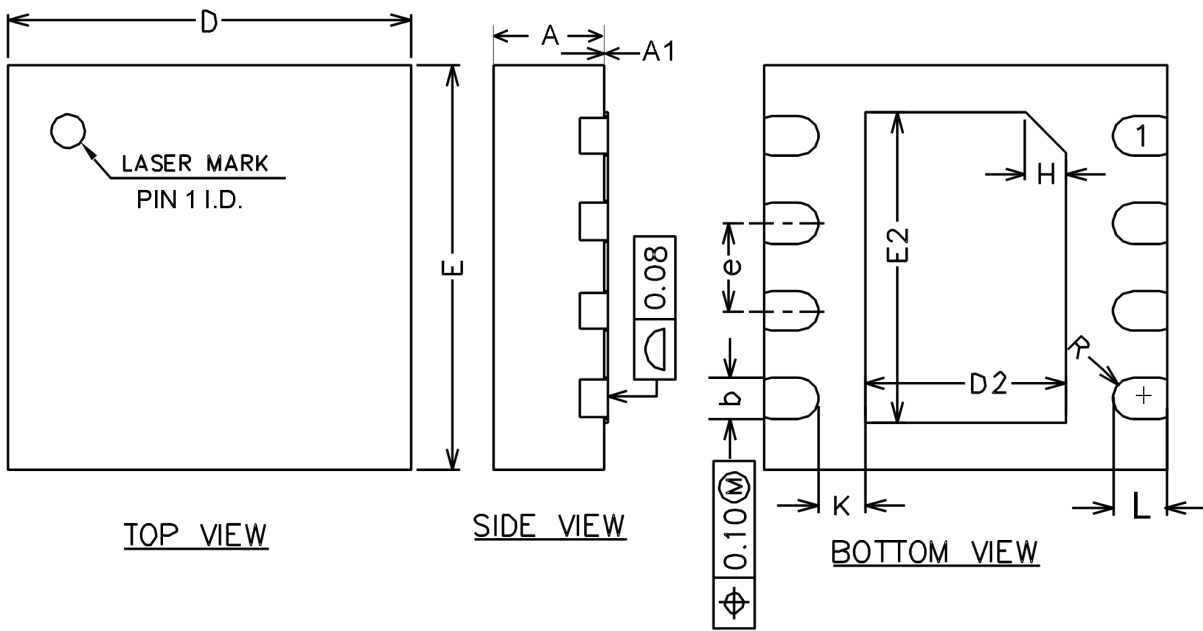
Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
K	0	-	0.25
L	0.30	0.40	0.60
L1	0.59 REF		
L2	0.25 BSC		
M	0.10	0.15	0.25
R	0.05	-	0.20
R1	0.05	-	0.20
Ø	0°	-	8°
Ø1	8°	10°	12°
Ø2	10°	12°	14°

Physical Dimensions: DFN2*2-6



Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	1.50	1.60	1.70
e	0.55	0.65	0.75
K	0.15	0.25	0.35
L	0.20	0.25	0.30
H	0.20 REF		

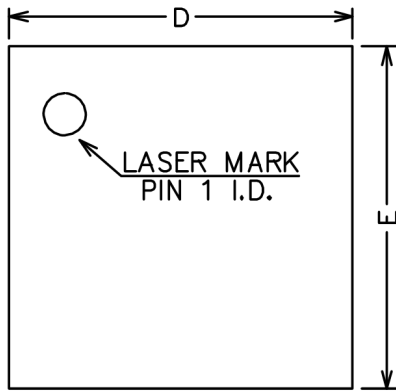
Physical Dimensions: DFN3*3-8



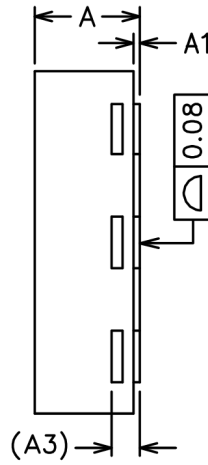
SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.30	0.35	0.40
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
H	0.30 REF		
K	0.20	0.30	0.40
L	0.30	0.40	0.50
R	0.16	-	-

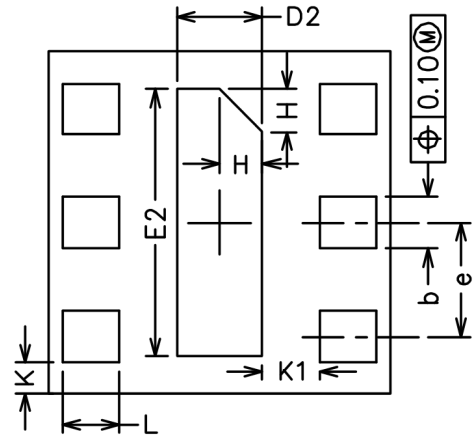
Physical Dimensions: DFN1.2*1.2-6



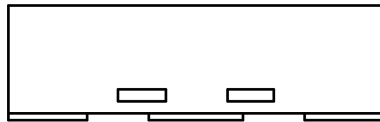
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3	0.10 REF		
b	0.13	0.18	0.23
D	1.10	1.20	1.30
E	1.10	1.20	1.30
D2	0.25	0.30	0.35
E2	0.89	0.94	0.99
e	0.30	0.40	0.50
H	0.15 REF		
K	0.11 REF		
K1	0.15	0.20	0.25
L	0.15	0.20	0.25



DIO7976

500 mA, Ultra-Low Noise and High PSRR LDO for RF and Analog Circuits

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