Automotive Multi-topology Controller IC

Features

- AEC-Q100 qualified
  - Device ambient temperature: -40°C ≤ T_A ≤ 125°C
  - Device junction temperature: -40°C ≤ T_J ≤ 150°C
- Wide input voltage: 4.5 V to 60 V
- Maximum output voltage is up to 60 V
- Enable function with very low shutdown current, < 15 μA at 105°C
- Multi-topology supported, Boost, Buck, Buck-Boost, SEPIC and Flyback
- Constant current or constant voltage regulation
- Switching frequency: 100 kHz to 500 kHz
- Optimized EMI performance
  - Spread spectrum: 7 kHz, ±15%
  - SYNC to external frequency
- Analog and PWM dimming (embedded or external) to adjust average LED current
- Diagnostic and protection
  - Open load, short to GND and open feedback detection
  - Output overvoltage protection
  - Input undervoltage protection
  - Overtemperature shutdown

Applications

- Automotive exterior lighting
- General illumination
- General DC-DC controller

Package Information

Part Number	Package	Body Size
DIA82901	EP-TSSOP14	5.0 mm × 4.4 mm

Description

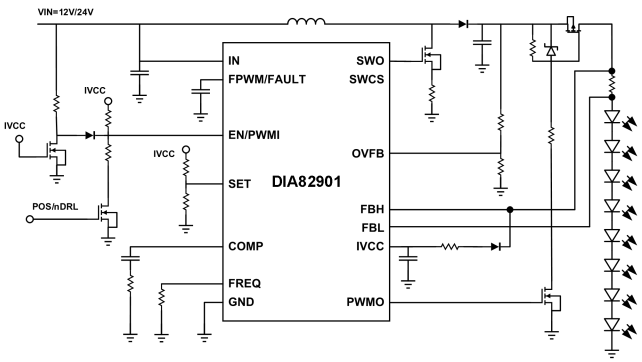
The DIA82901 is a multi-topology current mode DC-DC controller that supports Boost, Buck, Buck-Boost, SEPIC and Flyback. Flexible configuration in constant current/voltage and multi-topology make it ideal for automotive LED application.

The DIA82901 supports both analog dimming and PWM dimming. In addition to internal PWM dimming, embedded PWM dimming is supported, which can save the MCU resource. The device has very low shutdown current by enable function.

The switching frequency is adjustable from 100 kHz to 500 kHz or synchronized from 250 kHz to 500 kHz. The EMI performance of DIA82901 can be optimized by spread spectrum modulator.

The full diagnostic and protection are integrated, open circuit and short to GND detection, output overvoltage and input undervoltage protection, temperature shutdown. All these faults can be reported by FPWM/FAULT pin. In addition, the soft start function is integrated which limits the inrush current and voltage overshoot at start-up.

Simplified Schematic



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIA82901XT14	DIABG0A	3	Green	-40 to 125°C	EP-TSSOP14	Tape & Reel, 2500

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1. Pin Assignment and Functions

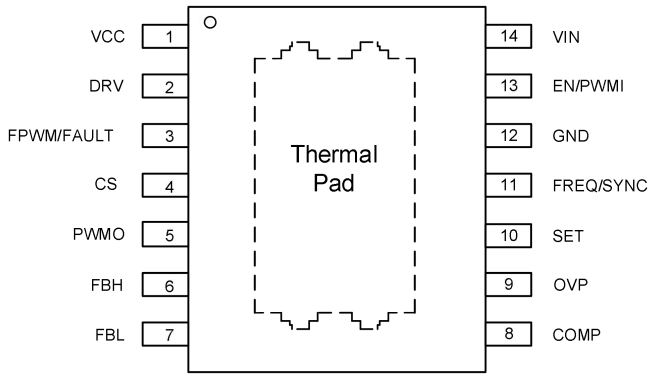


Figure 1. EP-TSSOP14 (Top view)

Pin No.	Name	Type	Description
1	VCC	O	Internal LDO. Used for internal biasing and gate drive. Bypass with external capacitor. Do not leave the pin open.
2	DRV	O	Switch gate driver. Connect the pin to gate of external switching MOSFET.
3	FPWM/FAULT	O	1. PWM frequency selector. Connect external capacitor to set PWM frequency. 2. 2. Pull high when fault (VCC_UVLO, OPEN, SHORT, TSD or OVP, FBH/FBL OVP) occurs; pull low when VIN_UVLO occurs.
4	CS	I	Current sense. Detects the peak current through switch.
5	PWMO	O	PWM dimming. Connect to gate of external MOSFET.
6	FBH	I	Voltage feedback positive. Non inverting input (+).
7	FBL	I	Voltage feedback negative. Inverting input (-).
8	COMP	I	Compensation. Connect RC network to the pin for control loop stability.
9	OVP	I	Overvoltage protection feedback. Connect to resistive voltage divider to set overvoltage threshold.
10	SET	I	Analog dimming. Load current adjustment pin. Do not leave the pin open. If analogy dimming feature is not used, connect the pin to VCC pin.
11	FREQ/SYNC	I	Frequency select or synchronization. Connect external resistor to GND to set frequency (two resistor sets are defined for activating or deactivating the spread spectrum modulator).
12	GND	G	Ground. Connect to system ground.
13	EN/PWMI	I	Enable or PWM. Apply logic “low” signal to disable device and put it in low current consumption. Apply logic “high” signal to enable device or PWM signal for dimming LED. Apply an analog signal (in a proper range) to enable a PWM engine which works at a defined duty cycle.
14	VIN	I	Supply. Supply for internal biasing.
	Thermal pad	-	Thermal pad. Connect to external heat spreading GND Cu area (for example, inner GND layer of multilayered PCB with thermal vias).

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
	Voltage range on OVP, CS, DRV, FPWM/FAULT, COMP, FREQ/SYNC, PWMO, VCC	-0.3 to 5.5	V
V_{IN}	Supply input voltage	-0.3 to 60	V
V_{SET}	SET	-0.3 to 60	V
V_{EN}	Enable or PWM input voltage	-40 to 60	V
V_{FBH} - V_{FBL}	Feedback error amplifier differential	-40 to 60	V
V_{FBH}, V_{FBL}	Feedback error amplifier inputs	-40 to 60	V
I_{FBH}, I_{FBL}	FBH and FBL current feed back error amplifier inputs ($t < 100$ ms, V_{FBH} - V_{FBL} = 0.3 V)	1	mA
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{IN}	Extended supply voltage range	4.5 to 60	V
V_{FBH}, V_{FBL}	Feedback voltage input	3 to 60	V
T_J	Junction temperature	-40 to 150	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
Human-body model	AEC-Q100-002	±2000	V
Charged-device model	AEC-Q100-011	±750	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53	°C/W

6. Electrical Characteristics

The values are obtained under V_{IN} = 8 V to 34 V, T_J = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Switching regulator						
V_{REF}	Feedback reference voltage	V_{REF} = V_{FBH} -$V_{FBL;}$ V_{SET} = 5 V; I_{LED} = 350 mA; Differential signal (not referred to GND)	0.29	0.30	0.31	V
V_{REF}	Feedback reference voltage	V_{REF}= V_{FBH} -V_{FBL}; V_{SET} = 0.4 V; I_{LED} = 70 mA; Differential signal (not referred to GND)	0.057	0.06	0.063	V
V_{REF_offset}	Feedback reference voltage offset	V_{REF} = V_{FBH} - $V_{FBL;}$ V_{SET} = 0.1 V; V_{OUT} > $V_{IN;}$ Differential signal (not referred to GND)			5	mV
$(\Delta V_{REF}/V_{REF}) / \Delta V_{IN}$	Voltage line regulation	V_{IN} = 8 V to 19 V; V_{SET} = 5 V; I_{LED} = 350 mA			0.15	%/V
$(\Delta V_{REF}/V_{REF}) / \Delta I_{BO}$	Voltage load regulation	V_{SET} = 5 V; I_{LED} = 100 to 500 mA			5	%/A
V_{CS}	Switch peak overcurrent threshold	V_{FBH} = V_{FBL} = 5 V; V_{COMP} = 3.5 V	125	150	175	mV
$D_{MAX,fixed}$	Maximum duty cycle	Fixed frequency mode	91			%
$D_{MAX,sync}$	Maximum duty cycle	Synchronization mode	88			%
t_{SS}	Soft start ramp	V_{SET} = 5 V; V_{REF} rising from 5% to 95% of V_{REF} (typ)	350	1000	1500	µs
I_{FBH}	Feedback high input current	V_{FBH} - V_{FBL} = 0.3 V	38	46	54	µA
I_{FBL}	Feedback low input current	V_{FBH} - V_{FBL}= 0.3 V	15	21	27	µA
I_{CS}	Switch current sense input current	V_{CS} = 150 mV	10	50	100	µA
$V_{IN,off}$	Input undervoltage shutdown	V_{IN} decreasing	3.5		4.5	V
$V_{IN,on}$	Input voltage startup	V_{IN} increasing			4.85	V
Gate driver for external switch (1)						
$I_{DRV,SRC}$	Gate driver peak sourcing current	V_{DRV} = 1 V to 4 V; Current flows out of pin		380		mA
$I_{DRV,SNK}$	Gate driver peak sinking current	V_{DRV} = 4 V to 1 V		550		mA
$t_{R,DRV}$	Gate driver output rise time	$C_{L,DRV}$ = 3.3 nF; V_{DRV} = 1 V to 4 V		30	60	ns
$t_{F,DRV}$	Gate driver output fall time	$C_{L,DRV}$ = 3.3 nF; V_{DRV} = 4 V to 1 V		20	40	ns
V_{DRV}	Gate driver output voltage	$C_{L,DRV}$ = 3.3 nF	4.5		5.5	V
Oscillator						

f_{FREQ}	Oscillator frequency	R_{FREQ} = 33 kΩ	250	300	350	kHz
f_{FREQ}	Oscillator frequency adjustment range		100		500	kHz
I_{FREQ}	FREQ/SYNC supply current	V_{FREQ} = 0 V			3	mA
V_{FREQ}	Frequency voltage	R_{FREQ} = 33 kΩ (f_{FREQ} = 300 kHz)	0.56	0.6	0.64	V
Synchronization						
f_{SYNC}	Synchronization frequency capture range		250		500	kHz
$V_{SYNC,H}$ (1)	Synchronization signal high logic level valid	Synchronization of external PWM “on” signal to falling edge	3.0			V
$V_{SYNC,L}$ (1)	Synchronization signal low logic level valid	Synchronization of external PWM “on” signal to falling edge			0.8	V
$t_{SYNC,PWM}$ (1)	Synchronization signal logic high pulse width	Synchronization of external PWM “on” signal to falling edge	200			ns
Spread spectrum modulator						
f_{FM} (1)	Modulation frequency	1.5 kΩ ≤ R_{FREQ} ≤ 9 kΩ		7		kHz
f_{DEV} (1)	Modulation depth	Related to switching frequency f_{FREQ} 1.5 kΩ ≤ R_{FREQ} ≤ 9 kΩ		±15		%
Enable / PWM input						
$V_{EN/PWMI,ON}$	Enable/PWMI turn on threshold		3			V
$V_{EN/PWMI,OFF}$	Enable/PWMI turn off threshold				0.8	V
$I_{EN/PWMI,H}$	Enable/PWMI high input current	$V_{EN/PWMI}$ = 16.0 V			100	μA
$I_{EN/PWMI,L}$	Enable/PWMI low input current	$V_{EN/PWMI}$ = 0.5 V		0.1	1	μA
$t_{EN,OFF,DEL}$	Enable turn off delay time		8	10	12	ms
$t_{PWMI,H}$	Minimum PWMI duty time		6			μs
$t_{EN,START}$ (1)	Enable startup time		100			μs
$V_{EN/PWM,DC\_0}$	PWM engine min voltage	PWM engine sets DC PWMO = 0%	0.313× V_{CC}	0.32 × V_{CC}		V
$V_{EN/PWM,DC\_100}$	PWM engine max voltage	PWM engine sets DC PWMO = 100%		0.56 × V_{CC}	0.571× V_{CC}	V
$DC_{PWMO,DC\_10\%}$	PWM engine DC	$V_{EN/PWM}$ = 0.344 × V_{CC}	8.5	10	11.5	%
f_{PWMO} (1)	PWM frequency range		100		500	Hz
R_{EN_INT} (1)	Enable/PWMI internal pull-down resistor	$V_{EN/PWMI}$ = 1.5 V to 3 V	0.7	1.35	2	MΩ
I_{FPWM_CH} (1)	FPWM/FAULT charging current		-150	-200	-250	μA
I_{FPWM_DIS} (1)	FPWM/FAULT discharging current		150	200	250	μA

V_{FPWM_H} (1)	FPWM/FAULT voltage rising threshold		1.9	2	2.1	V
V_{FPWM_L} (1)	FPWM/FAULT voltage falling threshold		0.9	1	1.1	V
V_{FPWM}	FPWM/FAULT output voltage with fault	I_{source} = 2 mA	4			V
f_{PWMO} (1)	PWM frequency	C_{FPWM} = 560 pF	265	350	435	Hz
Gate driver for dimming switch (1)						
$I_{PWMO,SRC}$ (1)	PWMO gate driver peak sourcing current	V_{PWMO} = 1 V to 4 V; Current flows out of pin		230		mA
$I_{PWMO,SNK}$ (1)	PWMO gate driver peak sinking current	V_{PWMO} = 4 V to 1 V		370		mA
Enable and dimming (1)						
$t_{R,PWMO}$	PWMO gate driver output rise time	$C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 1 V to 4 V		50	100	ns
$t_{F,PWMO}$	PWMO gate driver output fall time	$C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 4 V to 1 V		30	60	ns
V_{PWMO}	PWMO gate driver output voltage	$C_{L,PWMO}$ = 3.3 nF	4.5		5.5	V
Current consumption						
I_{Q_OFF}	Current consumption, shutdown mode	$V_{EN/PWMI}$ = 0.5 V; $T_J \leq$ 105°C; V_{IN} = 16 V			15	µA
I_{Q_ON}	Current consumption, active mode	$V_{EN/PWMI} \geq$ 4.75 V; R_{FREQ} = 33 kΩ; I_{BO} = 0 mA; V_{DRV} = 0% duty cycle; Dependency on switching frequency and gate charge of external switches			7	mA
Line regulator						
V_{CC}	Output voltage	6 V ≤ V_{IN} ≤ 45 V, 0.1 mA ≤ I_{CC} ≤ 40 mA	4.85	5	5.15	V
I_{LIM}	Output current limitation	V_{IN} = 13.5 V; V_{CC} = 4.5 V; Current flows out of pin	51		90	mA
V_{DR}	Dropout voltage	V_{IN} = 4.5 V; V_{CC} = 25 mA			0.5	V
$V_{CC,HDRM}$ (2) (3)	Undervoltage reset headroom	V_{CC} decreasing; V_{CC} - V_{CC_OFF}	100			mV
V_{CC_OFF} (4)	VCC undervoltage reset switch-off threshold	V_{CC} decreasing	3.6		4	V
V_{CC_ON}	VCC undervoltage reset switch-on threshold	V_{CC} increasing			4.5	V
Short circuit protection						
V_{FBL,FBH_S2G}	FBH and FBL short circuit fault sensing common mode range	V_{FBH} = V_{FBL} decreasing	1.5		2	V

Temperature protection (1)						
$T_{J,SD}$	Overtemperature shutdown		160	170	180	°C
$T_{J,SD,HYST}$	Overtemperature shutdown hysteresis			15		°C
Overvoltage protection						
$V_{OVP,TH}$	Output overvoltage feedback threshold increasing		1.21	1.25		V
$V_{OVP,HYS}$ (1)	Output overvoltage feedback hysteresis	Output voltage decreasing	50		150	mV
t_{OVPRR}	Overvoltage reaction time	Output voltage decreasing	2		10	μs
I_{OVP}	Overvoltage feedback input current	V_{OVP} = 1.25 V	-1	0.1	1	μA
Open load and open feedback diagnostics						
$V_{REF,1,3}$	Open load/feedback threshold	$V_{REF} = V_{FBH} - V_{FBL}$; Open circuit 1 or 3	-100		-20	mV
$V_{REF,2}$	Open feedback threshold	$V_{REF} = V_{FBH} - V_{FBL}$; Open circuit 2	0.5		1	V
FBH/FBL OVP						
$V_{FB,OVP}$(1)	FBH/FBL overvoltage threshold			75		V
Analog Dimming						
V_{SET} (1)	SET programming range		0		1.6	V

Note:

(1) Guaranteed by design.

(2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

(3) If embedded PWM engine is used, a 4.7 μF value has to be chosen as a minimum.

(4) Selection of external switching MOSFET is crucial and the $V_{CC\_OFF\ min}$ as worst case the threshold voltage of MOSFET must be considered.

(5) It is recommended that the chip peripheral capacitance parameters VCC Buffer Capacitor(C_{CC}) and VCC Buffer Capacitor ESR($R_{CC,ESR}$) meet the following requirements: 0.47 μF ≤ C_{CC} ≤ 100 μF, $R_{CC,ESR}$ ≤ 0.5 Ω.

(6) Specifications subject to change without notice.

7. Block Diagram

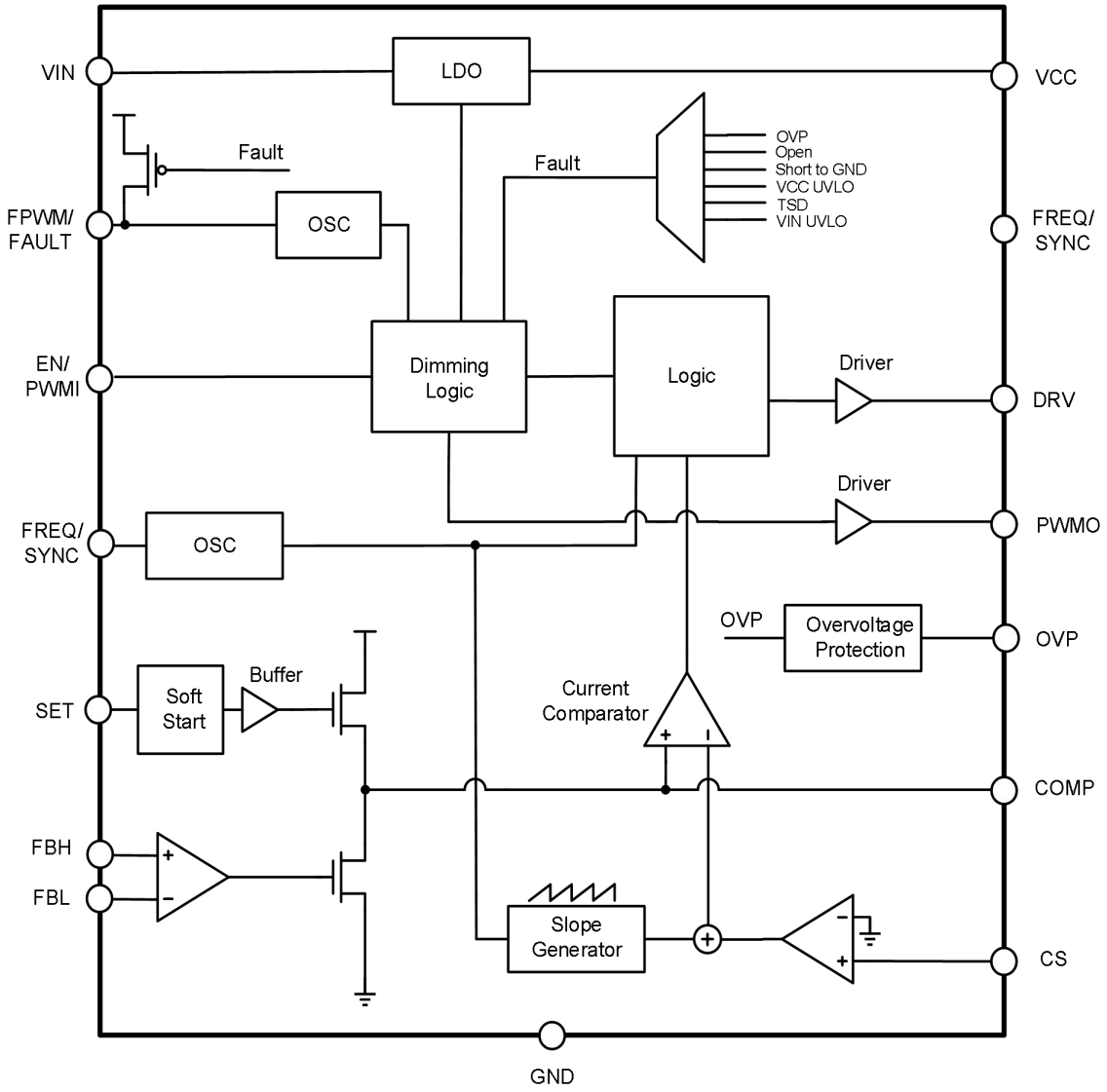


Figure 2. Block diagram

8. Function Description

8.1. Switching regulator

The DIA82901 regulator is suitable for boost, buck, buck-boost, sepic and flyback configurations. The constant output current is especially great for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

To determine the appropriate pulse width duty cycle (on time) for constant output current, the switching current mode controller adopts the peak current through the external power switch and error in the output current. A modulated signal to an internal gate driver is provided by the current mode controller, and it drives an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has integrated internally slope compensation, preventing sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty). The DIA82901 also features an integrated soft start which limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} so as to minimize potential overvoltage at the output.

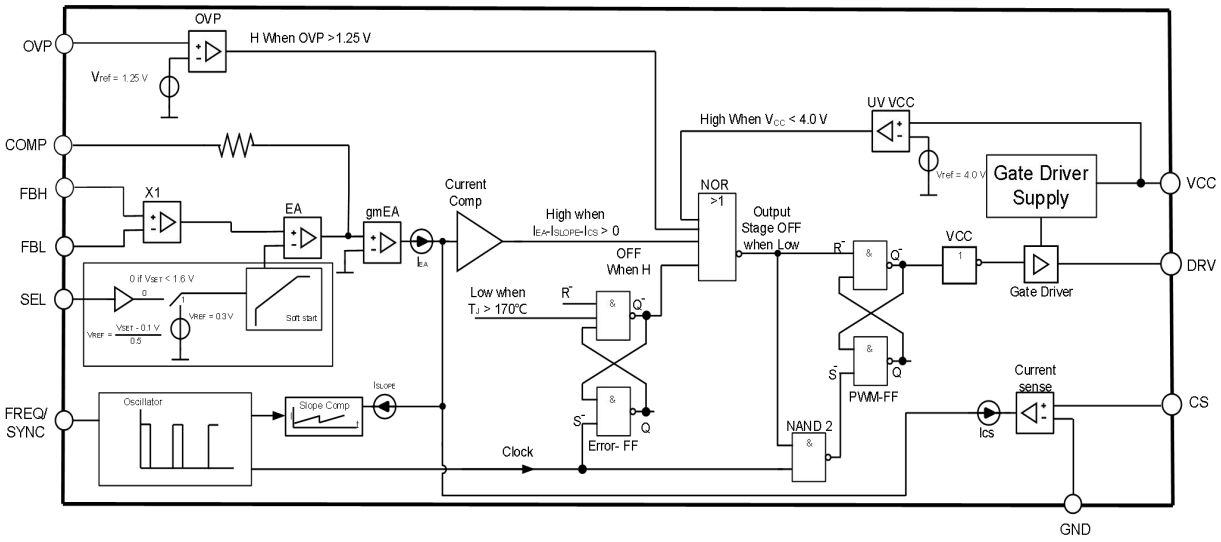


Figure 3. Switching regulator block diagram

8.2. Switching oscillator and synchronization

8.2.1. RFREQ vs. switching frequency

The internal oscillator of the DIA82901 can determine the switching frequency of the regulator. An external resistor referred to GND can be used to select the switching frequency ranging from 100 kHz to 500 kHz and the status of spread spectrum modulator can be selected.

The range scale of the usable resistor is divided in two sections.

For lower values of resistor it selects the switching frequency with the spread spectrum modulator “on”, while for higher values of the range it selects the switching frequency with the spread spectrum modulator “off”.

To set the desired switching frequency with spread spectrum modulator “off”, the external resistor value is calculated by the following equation and is summarized in Table 1.

$$R_{FREQ\ —\ SSMoff} = \frac{1}{(340 \times 10^{-12} \times f_{FREQ})^{1.13}} \quad (1)$$

To set the desired switching frequency with spread spectrum modulator “on”, the external resistor value is calculated by the following equation.

$$R_{FREQ\ —\ SSMon} = \frac{1}{(600 \times 10^{-12} \times f_{FREQ})^{0.934}} - (600) \quad (2)$$

What’s more, the oscillator is able to change from the frequency set by the external resistor to a synchronized frequency from an external clock source. If the pin FREQ/SYNC provides an external clock source, the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture ranges from 250 kHz to 500 kHz.

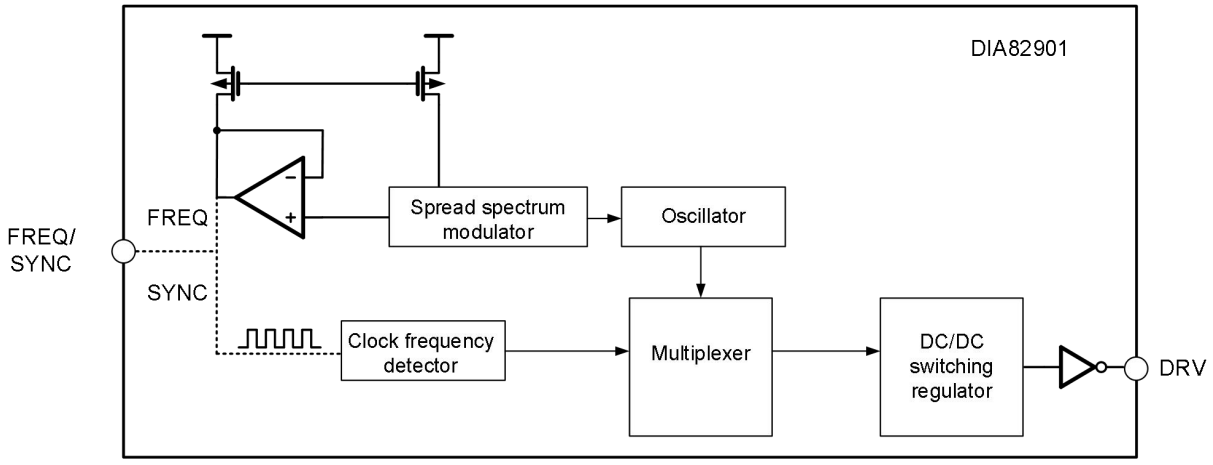


Figure 4. Oscillator and synchronization block diagram

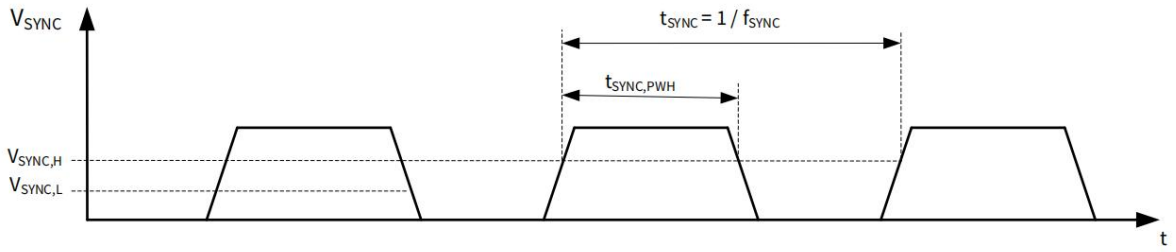


Figure 5. Synchronization timing diagram

Table 1. R_{FREQW} vs. f_{SW}

Spread spectrum	R_{FREQW}	f_{SW}
Spread spectrum On	1.8 kΩ	435 kHz
	2.2 kΩ	370 kHz
	2.7 kΩ	311 kHz
	3.3 kΩ	260 kHz
	3.9 kΩ	224 kHz
	4.7 kΩ	188 kHz
	5.6 kΩ	159 kHz
	6.8 kΩ	132 kHz
	8.2 kΩ	110 kHz
Spread spectrum Off	22 kΩ	422 kHz
	27 kΩ	352 kHz
	33 kΩ	295 kHz
	39 kΩ	254 kHz
	47 kΩ	216 kHz
	56 kΩ	185 kHz
	68 kΩ	156 kHz
	82 kΩ	132 kHz

8.2.2. Spread spectrum

In the lower frequency range of the spectrum (for example, f < 30 MHz), the spread spectrum modulation technique greatly improves the EMI performance.

The spread spectrum approach may be used to improve the input and output filters to meet EMC requirements. Furthermore, because the input capacitor series resistor is necessary for the low frequency filter characteristic, the need for low ESR input capacitors is reduced. If average restrictions are strictly enforced, this can be advantageous economically.

The modulation frequency f_{FM} is internally fixed, while the modulation depth is a fraction of the switching frequency f_{DEV}.

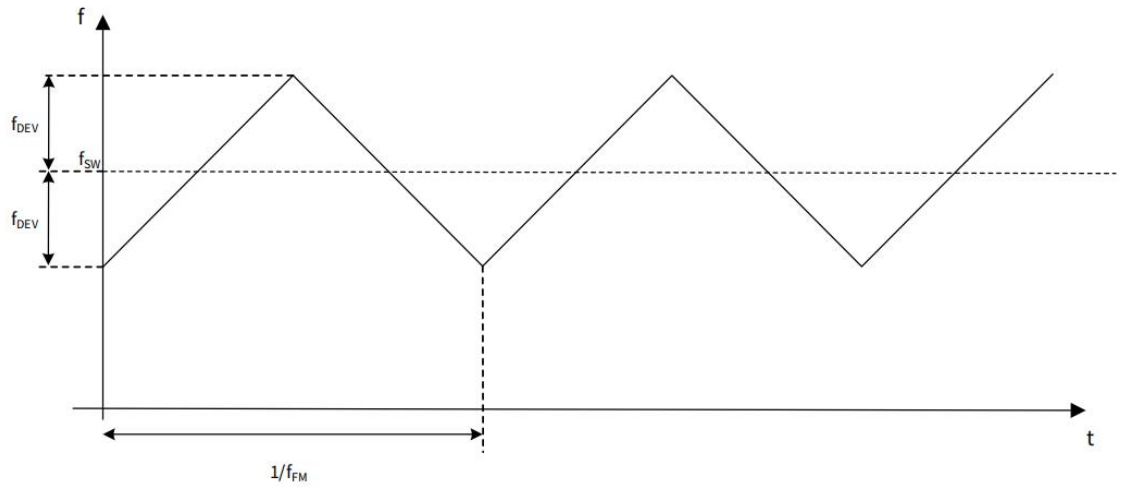


Figure 6. Spread spectrum modulator

8.3. Enable & Dimming function

The enable and dimming functions of the DIA82901 will be affected by The status of the pin EN / PWMI. For different values of the voltage on this pin, the device has different behaviors as below:

- When $V_{EN/PWMI} < V_{EN/PWMI,OFF}$ (= a valid logic “low” is present), the device is powered off;
- When $V_{EN/PWMI} > V_{EN/PWMI,ON}$ (= a valid logic “high” is present), the device is powered on and it can accept a digital PWM;
- When an analog signal is in between $V_{EN/PWMI,DC\_0}$ and $V_{EN/PWMI,DC\_100}$, the device and the embedded PWM engine are powered on.

8.3.1. Enable function

The enable function determines whether the device is on or off. When the device is at the start-up status or when a valid logic low signal on enable pin EN / PWMI for a time longer than $t_{EN,OFF,DEL}$ powers off the device, the current consumption is less than I_{Q_OFF}.

To fully activate the DIA82901 at the start-up status, a valid logic “high” need to be present while the VCC reaches the level V_{CC_ON}.

To achieve the enable function, the DIA82901 has integrated a pull down resistor . If the EN pin is left open, this pull down resistor, R_{EN_INT}, makes sure that the IC is shut down and the power switch is off.

8.3.2. Digital PWM dimming function

If a valid logic high/low pattern is present on EN / PWMI, the digital PWM dimming function is activated. The EN / PWMI signal sets the average current on the load, enabling and disabling the gate drivers according to the logic signal present in the pin.

The DIA82901 distinguishes between the enable off and PWM dimming signal when PWM logic is engaged by requiring the enable off at the EN/PWMI pin to remain low for the Enable turn off delay time. Find the details of the pattern and the timing constraints in the below figure.

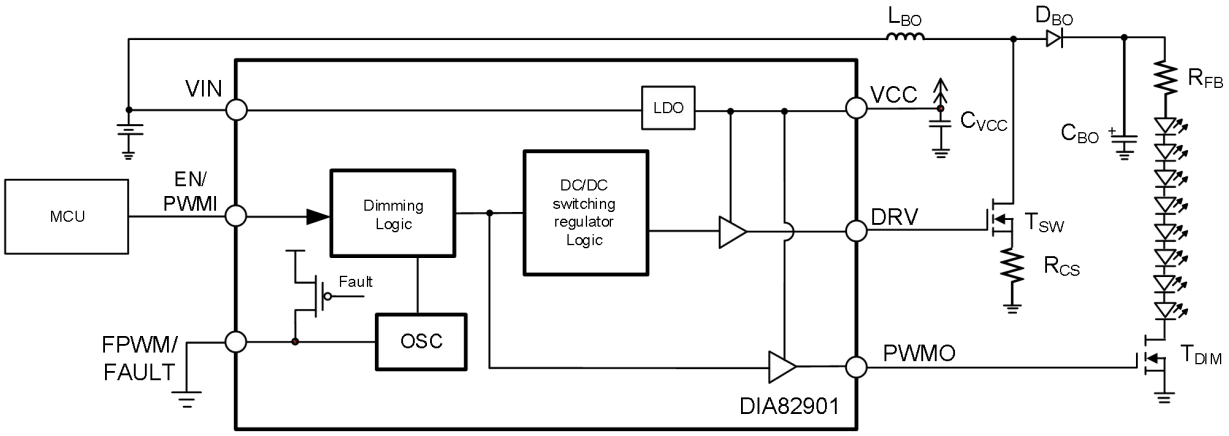


Figure 7. Block diagram and simplified application circuit enable and LED dimming

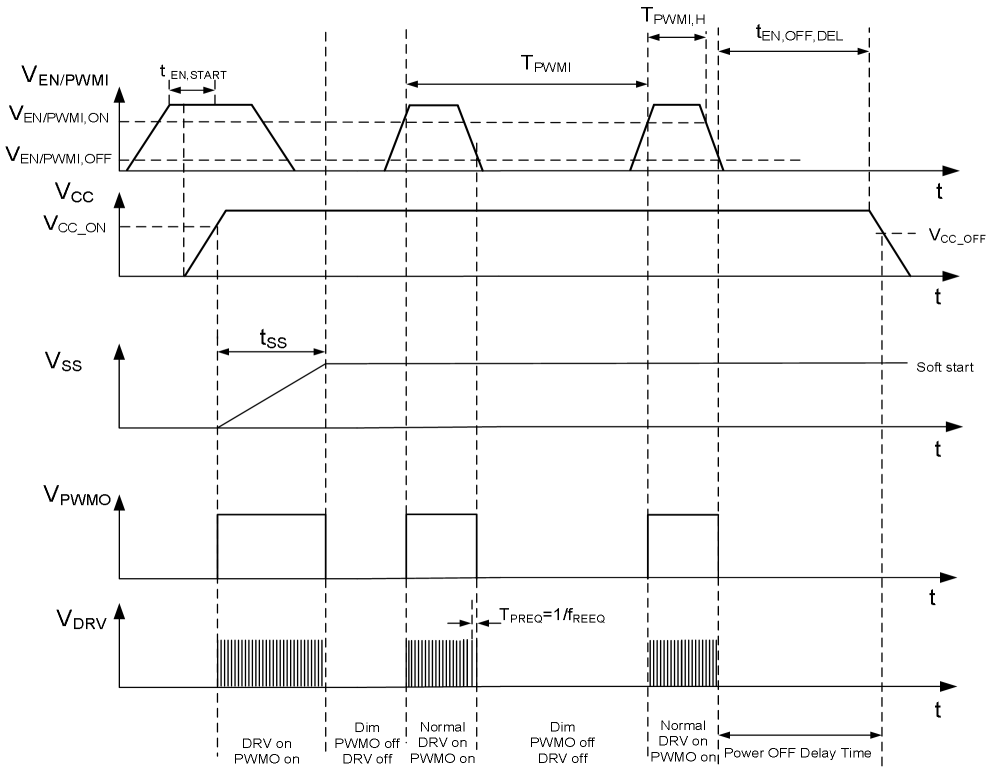


Figure 8. Timing diagram enable and LED dimming

Note: The slope of the V_{CC} is related to the filter capacitor. So its steady state condition can be achieved after $t_{EN,START}$.

8.3.3. Embedded PWM dimming function

In the voltage window in between a valid logic “low” level and a valid logic “high” level, the embedded PWM dimming function (PWM engine) is activated. According to the analog voltage of the pin, a duty cycle (DC) on PWMO output is generated in this voltage window. The equation (3) show how to get the DC value:

$$DC[\%] = \frac{V_{EN/PWMI} - 0.32 \times V_{CC}}{0.24 \times V_{CC}} \times 100[\%] \quad (3)$$

About the calculation of the $V_{EN/PWMI}$, the pull-down resistor is involved and the resistor features the shut down when the pin EN is left open. If this value is considered and a voltage divider between VCC and ground is used, the DC can be calculated by the equation (4):

$$DC[\%] = \frac{\frac{R_B \,||\, R_{EN\_INT}}{R_B \,||\, R_{EN\_INT} + R_A} - 0.32}{0.24} \times 100[\%] \quad (4)$$

The frequency of PWMO signal varies with the value of the capacitor on the pin FPWM/FAULT. Two internal current generators charge and discharge the capacitor and this signal supplies an internal divider to produce the desired frequency.

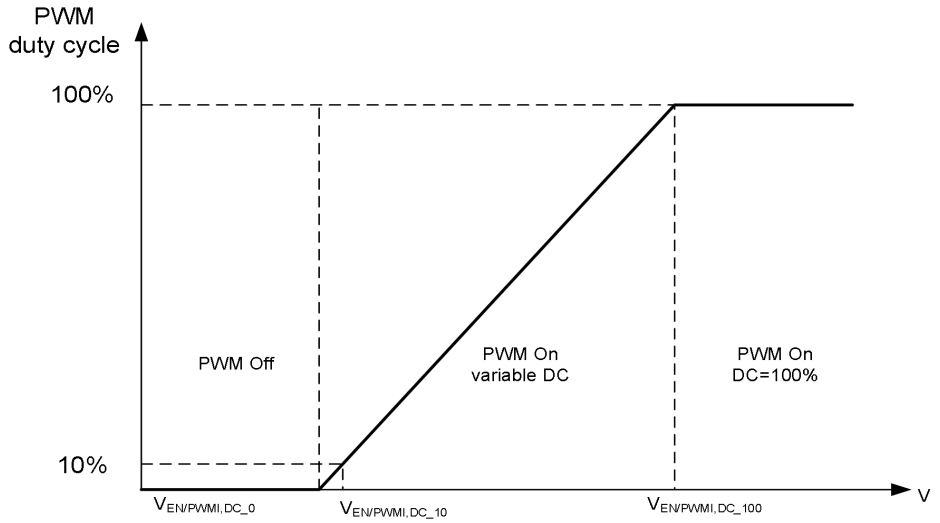


Figure 9. Duty cycle variation as a function of $V_{EN/PWMI}$

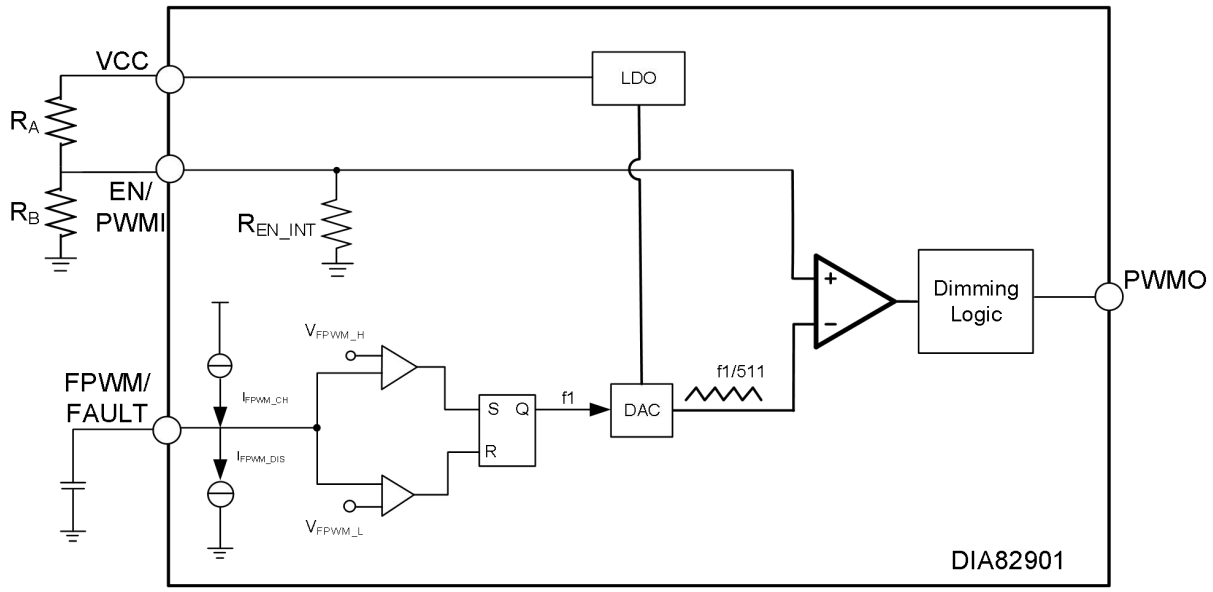


Figure 10. Block diagram of PWM engine

The following equation shows the relation of PWM frequency and the capacitor:

$$f_{PWMO} = \frac{1}{511 \times C_{FPWM} \times (V_{FPWM\_H} - V_{FPWM\_L}) \times (\frac{1}{|I_{FPWM\_CH}|} + \frac{1}{|I_{FPWM\_DIS}|})} \quad (5)$$

Typically, the variation of PWM frequency is shown in Figure 11. DIOO recommends to put this capacitor very close to the pin FPWM/FAULT so as to decrease the impact of parasitic capacitance as much as possible. The signal produced by the PWM engine (with the desired DC and frequency) is capable of enabling and disabling the gate drivers and modulating the average current on the load.

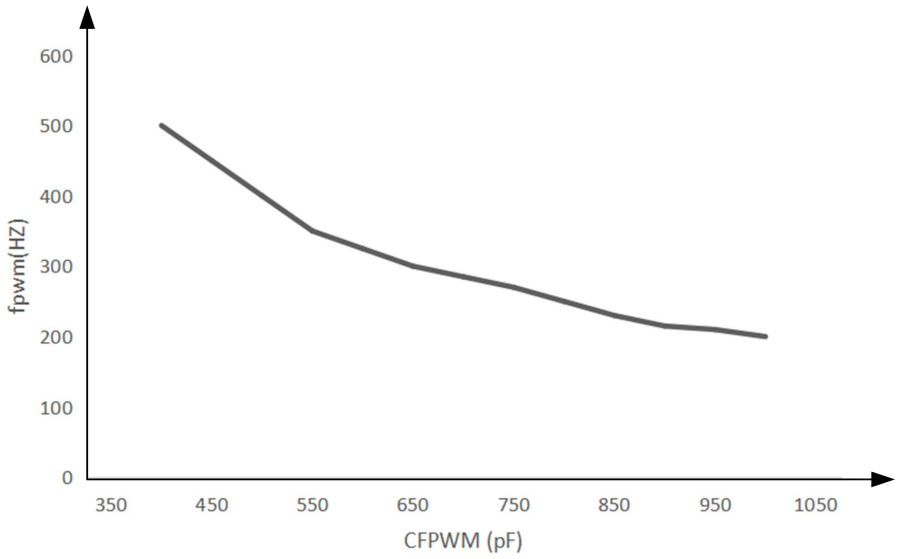


Figure 11. PWM frequency variation as a function of C_{FPWM}

To activate the internal logic, it's only in the start-up status that a valid logic high on the pin EN/PWMI is needed. The valid logic high on pin EN/PWMI has to remain until V_{CC} reaches its steady state. A proposal circuit to obtain this behavior is shown in Figure 12.

It acts as below:

- At start-up Q1 is off and VIN supplies pin EN / PWMI through R_{LIM} and it starts up the circuit;
- When the DIA82901 is ready to work (for example, the VCC has reached its steady state), the VCC switches on Q1 (the current through Q1 is limited by R_{LIM});
- Then the voltage on EN / PWMI pin given by the resistor divider R_A, R_B provides the desired duty cycle.

The diode D1 ensures the proper behavior for the biasing.

Only when embedded PWM dimming function is used, this start-up circuit is needed. To ensure the start-up of the device, the suitable dimensioning of R_{LIM} and voltage divider (R_A and R_B) resistors is needed . $V_{EN/PWMI}$ has to be higher than $V_{EN/PWMI,ON}$ during start-up. Fixing R_{LIM}, R_B can be calculated by following equation:

$$R_B > \frac{V_{EN/PWMI,\ ON}}{V_{IN} - V_{D1} - V_{EN/PWMI,\ ON}} \times R_{LIM} \quad (6)$$

The value of R_A has to be calculated based on the desired duty cycle.

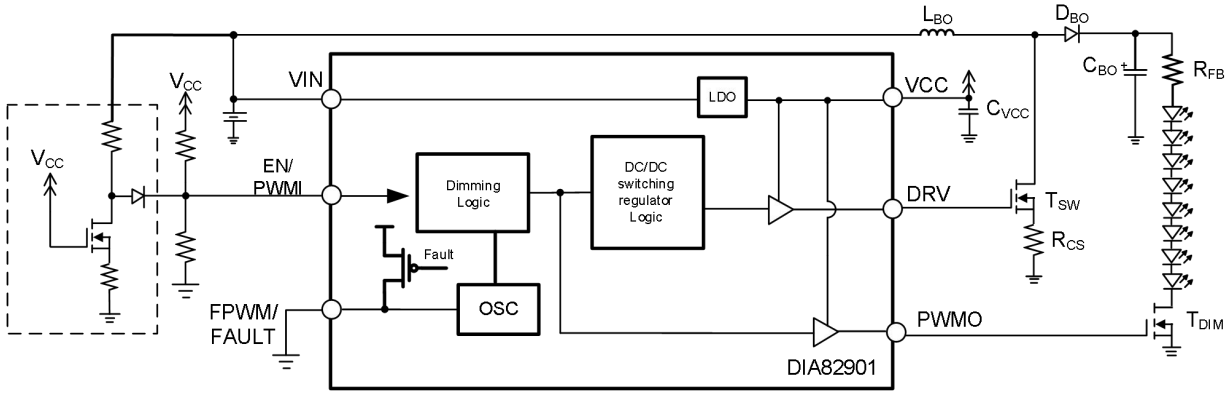


Figure 12. Block diagram of analog PWM dimming with simplified application circuit

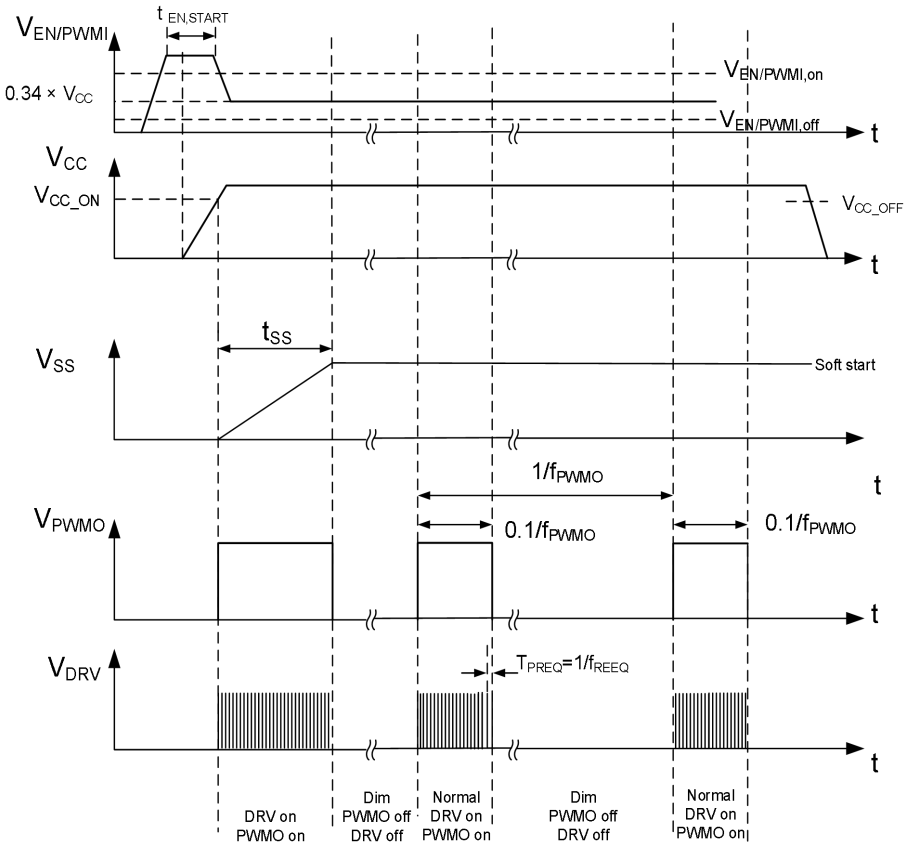


Figure 13. Timing diagram enable and LED dimming with PWM engine

8.4. FPWM/FAULT indicator

The devices allow the FPWM/FAULT pin to indicate fault conditions.The FPWM/FAULT pin goes high under the following conditions: VCC_UVLO, OPEN, SHORT, TSD, OVP Feedback or FBH/FBL OVP.

8.5. Linear regulator

The internal linear voltage regulator supplies the internal gate drivers with a voltage of 5 V (typ) and current up to $I_{LIM,min}$ For stability and buffering transient load currents, it's needed to have an external output capacitor with ESR lower than $R_{CC,ESR}$ on pin VCC.

During normal operation, the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. The output capacitor with a proper size must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

8.5.1. Integrated undervoltage protection for the external switching MOSFET

In case the output voltage falls below the VCC undervoltage reset switch off threshold (V_{CC_OFF}), an integrated undervoltage reset threshold circuit is capable of monitoring the linear regulator output voltage (V_{CC}) and resets the device. Through the way of making sure that the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET, the undervoltage reset threshold for the VCC pin can protect the external switches from excessive power dissipation.

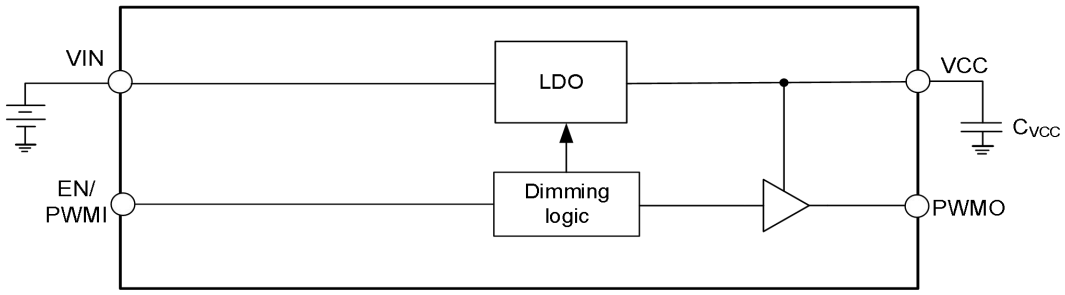


Figure 14. Voltage regulator block diagram and simplified application circuit

8.6. Protection and diagnostic functions

The integrated circuits of the device can diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. Furthermore, the FBH and FBL potential is monitored and in case the LED load is shorted to GND (See Figure 20) and the regulator stops the operation and protects the system. In case any of the six fault conditions occur the PWMO and DRV signal will change to an active logic “low” signal to communicate that a fault has occurred, while VCC shutdown occurs only in case of overtemperature or input undervoltage (See Figure 15 and Table 2). The various open load and open feedback conditions is shown in Figure 16.

If there’s an overtemperature condition, the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical value of junction shutdown temperature is 170°C. The IC will automatically restart after cooling down. The DIA82901 has integrated the thermal shutdown as a protection function, which can prevent IC destruction. It is not aimed at continuous use in normal operation (See Figure 18). To calculate the proper overvoltage protection resistor values (See Figure 19).

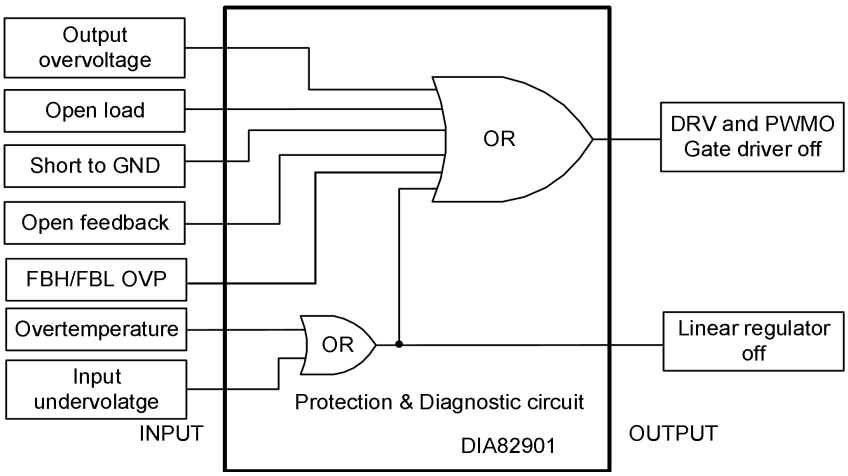


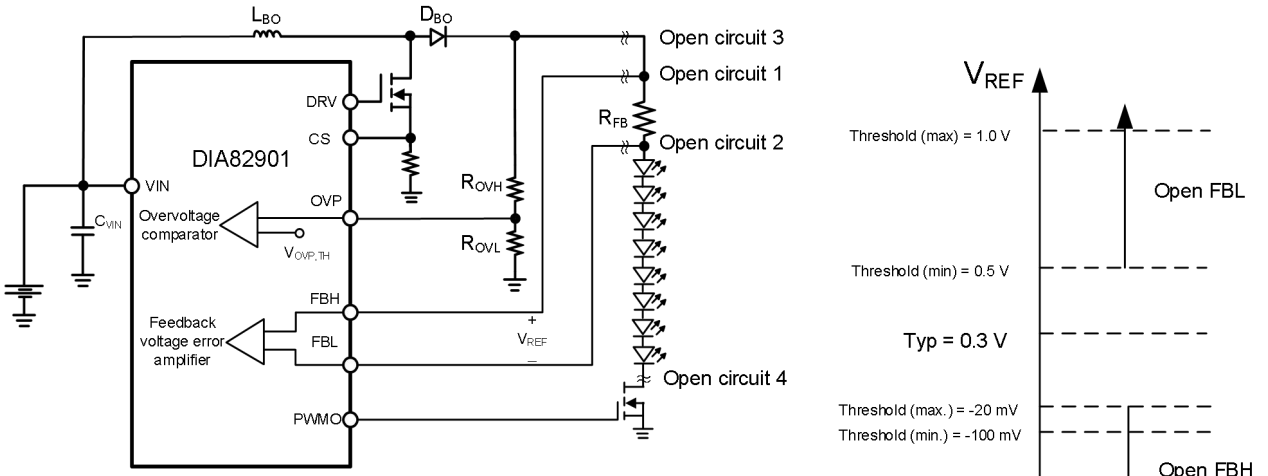
Figure 15. Protection and diagnostic function block diagram

Table 2. Diagnosis truth table(1)

Input		Output		
Condition	**Level**	**DRV**	**PWMO**	**VCC**
Overvoltage at output	False	SW	High or SW	Active
	True	Low	Low	Active
Open load	False	SW	High or SW	Active
	True	Low	Low	Active
Short to GND at LED chain	False	SW	High or SW	Active
	True	Low	Low	Active
Open feedback	False	SW	High or SW	Active
	True	Low	Low	Active
Overtemperature	False	SW	High or SW	Active
	True	Low	Low	Shutdown
Undervoltage at input	False	SW	High or SW	Active
	True	Low	Low	Shutdown
FBH/FBL OVP	False	SW	High or SW	Active
	True	Low	Low	Active

Note:

(1) SW = Switching; False = Condition does NOT exist; True = Condition does exist



Open circuit condition	Fault condition	Fault threshold voltage V_{REF}
1	Open FBH	-20 to -100 mV
2	Open FBL	0.5 to1.0 V
3	Open VBO	-20 to -100 mV
4	Open PWMO	Detected by overvoltage

Figure 16. Open load and open feedback conditions

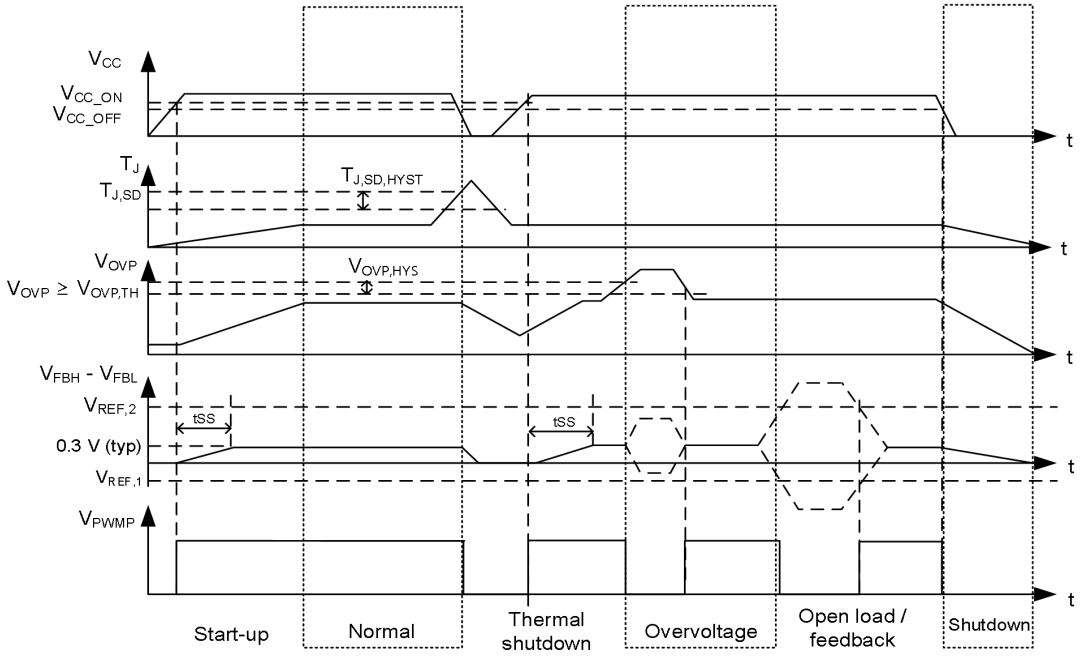


Figure 17. Open load, overvoltage and overtemperature timing diagram

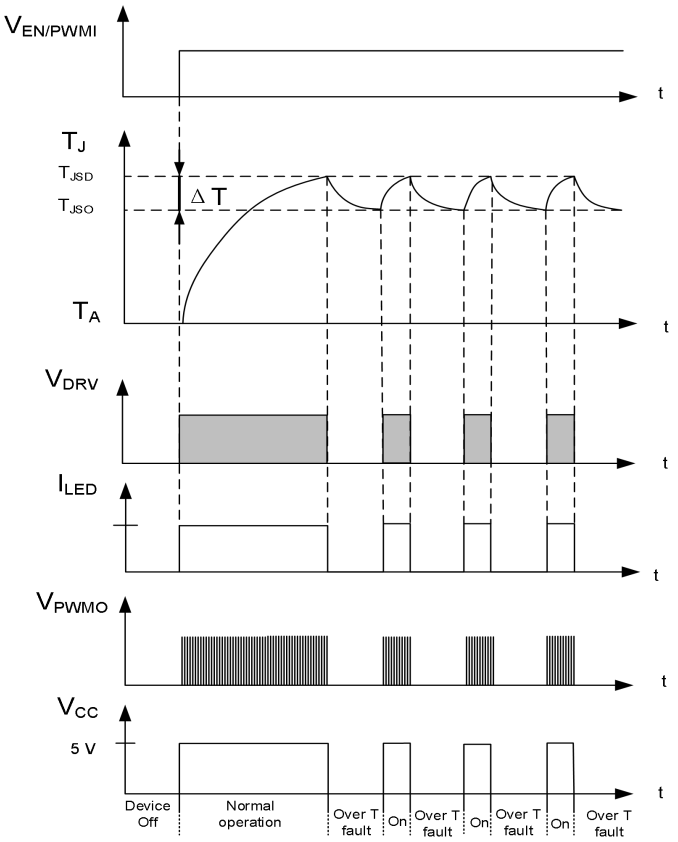


Figure 18. Device overtemperature protection behavior

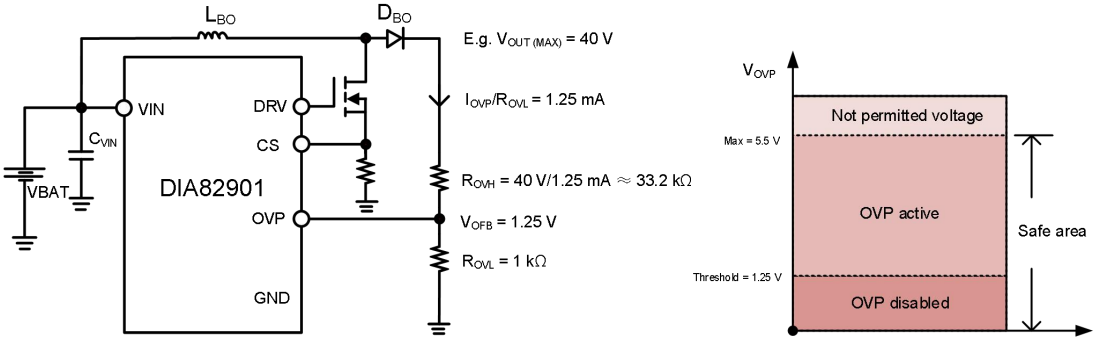


Figure 19. Overvoltage protection description

Short to GND protection for high-side return applications (B2B) from Figure 30 and Figure 31.

The FBH and FBL pins features a short to GND detection threshold (V_{FBL,FBH_S2G}). When the potential on these pins falls below this threshold, the device stops its operation. It will force the PWMO signal to change to inactive state (“low” potential) and the corresponding p-channel (T_{DIM2}) is switched off accordingly and protects the LED chain. For the B2B application some external components are needed to ensure a “low” potential during a short circuit event. D_1 and D_2 are low power diodes and the resistor R_{PROT} (10 kΩ) is required to limit the current through this path. The diode D_3 should be a high power diode and is required to protect the RFB, FBH and FBL pins when an short circuit to GND event occurs. This short circuit detection and protection concept considers potential faults for LED chains (LED modules) which are separated from the ECU through two wires (at the beginning and the end of the LED chain). If the short circuit condition disappears, the device will restart with a soft start.

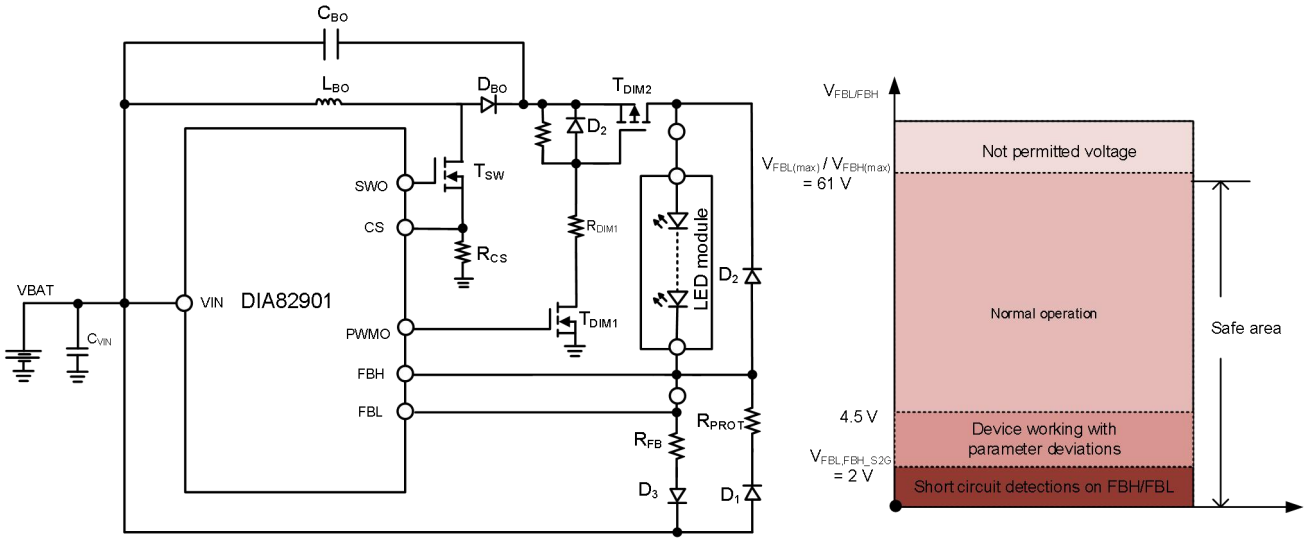


Figure 20. Short circuit to GND protection

8.7. Analog dimming

By generating an internal current based on its voltage (V_{SET}), the SET pin influences the feedback voltage error amplifier. If there's no need for the analog dimming feature, this pin must be tied to VCC or external voltage supply higher than 1.6 V. Find more details of different application scenarios below(See Figure 23). This pin can also go outside of the ECU for instance if a thermistor is connected on a separated LED module and the analog dimming input is used to thermally protect the LEDs. It's necessary to place an external series resistor to limit the current for reverse battery protection of this pin.

8.7.1. Analog dimming purpose

For LED manufacturers, it is difficult to deliver LEDs which have the same brightness, colorpoint and forward voltage class. Due to this relatively wide spread of the crucial LED parameters automotive customers order LEDs from one or maximum two different colorpoint classes. The LEDs must be preselected by the the LED manufacturer to deliver the requested colorpoint class. These preselected LEDs are matched in terms of the colorpoint but a variation of the brightness remains. An analog dimming feature is needed to correct the brightness deviation. This means LED current can be adjusted by applying an external voltage V_{SET} at the SET pin.

If the DC/DC application is separated from the LED loads the ECU manufacturers aim is to develop one hardware which should be able to handle various load current conditions (for example, from 80 mA to 400 mA) to cover different applications. The analog dimming is critical to achieve this average LED current adjustment.

8.7.2. Application example

The desired LED current is 400 mA. For the calculation of the correct feedback resistor R_{FB} the following equation can be used: This equation is valid if the analog dimming feature is disabled and V_{SET} > 1.6 V.

$$I_{LED} = \frac{V_{REF}}{R_{FB}} \rightarrow R_{FB} = \frac{V_{REF}}{I_{LED}} \rightarrow R_{FB} = \frac{0.3\ V}{400\ mA} = 750\ m\Omega \quad (7)$$

Related electrical parameter is ensured with V_{SET} = 5 V. By controlling V_{SET} between 0.1 V and 1.6 V, a decrease of the average LED current can be achieved. The mathematical relation can be calculated by the following equation:

$$I_{LED} = \frac{V_{SET} - 0.1\,V}{5 \times R_{FB}} \quad (8)$$

Refer to the concept drawing in Figure 22.

If V_{SET} ≤ 50 mV, the switching activity is stopped and I_{LED} = 0 A

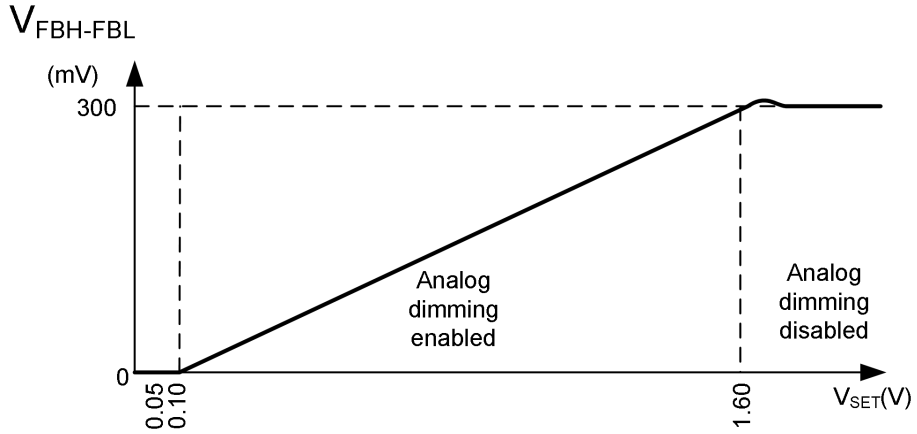


Figure 21. Basic relationship between V_{REF} and V_{SET} voltage

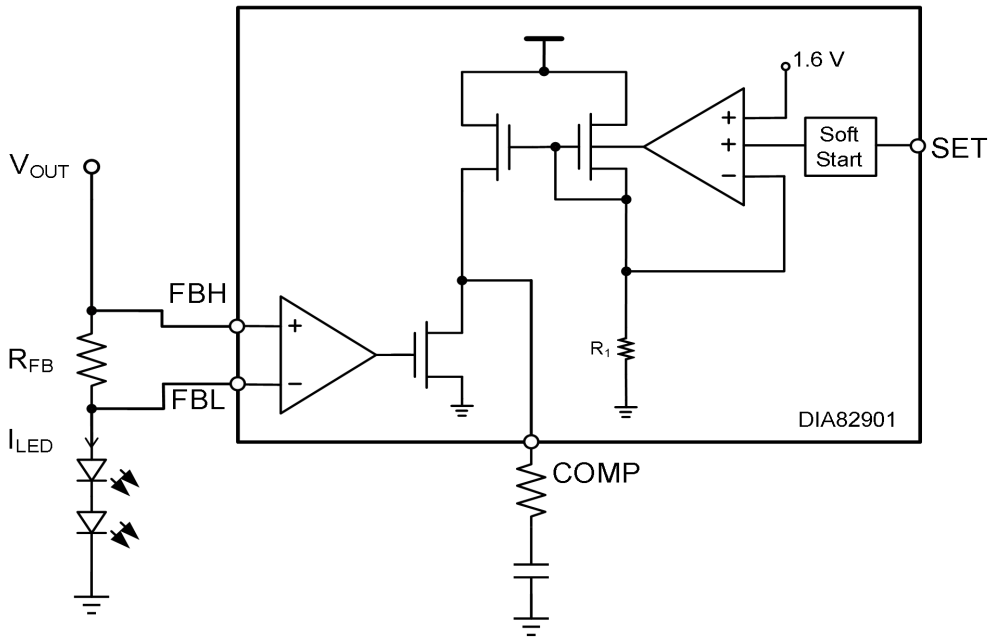


Figure 22. Concept drawing analog dimming

8.7.3. Multi-purpose usage of the analog dimming feature

- A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the DIA82901. If the current consumption is lower than 20 mA, the integrated voltage regulator, V_{CC}, can be used to supply the µC or external components.
- The analog dimming feature is directly connected to V_{IN}. In this configuration the LED current is reduced if V_{IN} is decreased. If V_{IN} drops to a lower potential, the DC/DC boost converter increases the duty cycle of DRVI. This leads to an increase of the input current consumption. If applications require a decrease of the LED current in respect to V_{IN} variations, then choose this setup.
- For systems without µC on board, it's a choice to use an external resistor divider connected between VCC (integrated 5 V regulator output and gate buffer pin) SET and GND. The concept allows to control the LED current via placing cheap low power resistors. In addition, a temperature sensitive resistor (thermistor) to protect the LED loads from thermal destruction can be connected.
- When there's no need for the analog dimming feature, the SET pin must be connected directly to higher than 1.6 V potential (for example, VCC potential)
- Instead of an DAC, the µC can give a PWM signal and an external R-C filter produces a constant voltage for the analog dimming. After reading the coding resistor placed at the LED module, the voltage level depends on the PWM frequency (f_{PWM}) and duty cycle (DC) which can be controlled by the µC software.

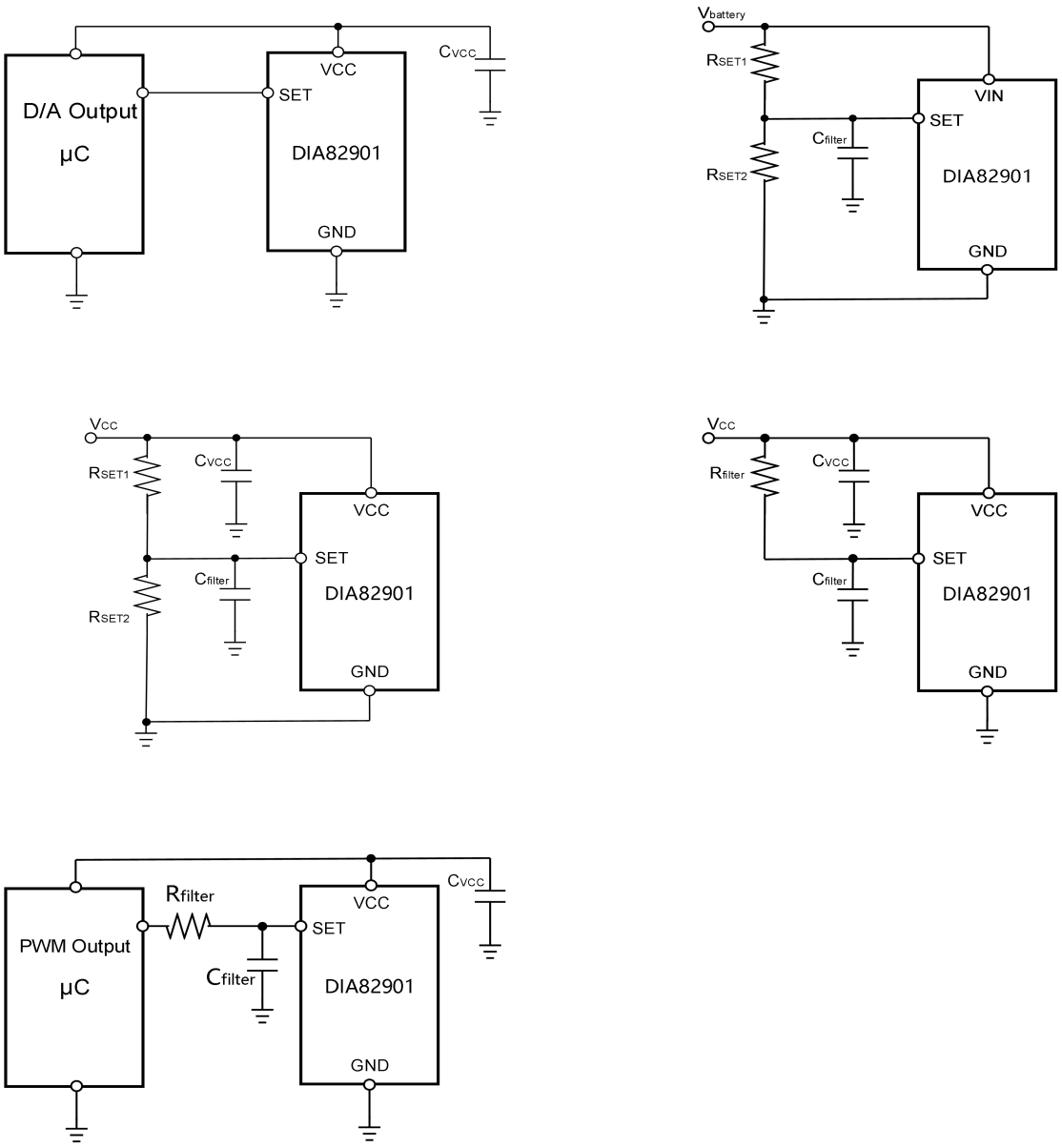


Figure 23. Analog dimming in various applications

9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

POS/nDRL is the signal that indicates which function is activated (position light or daytime running light).

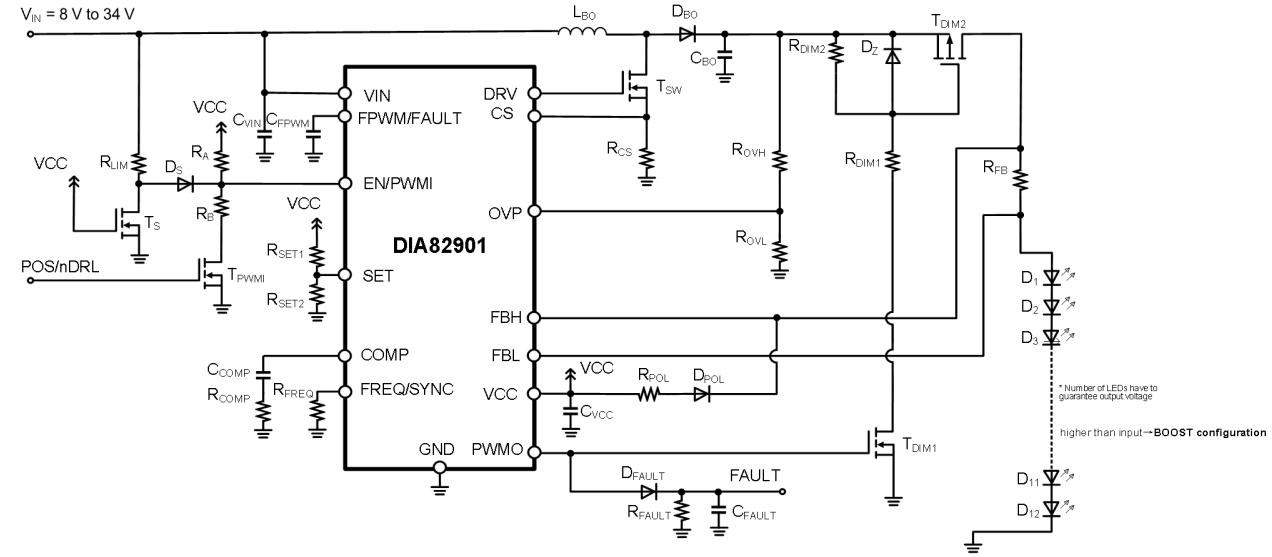


Figure 24. Boost to ground using embedded PWM engine application circuit - B2G (Boost configuration)

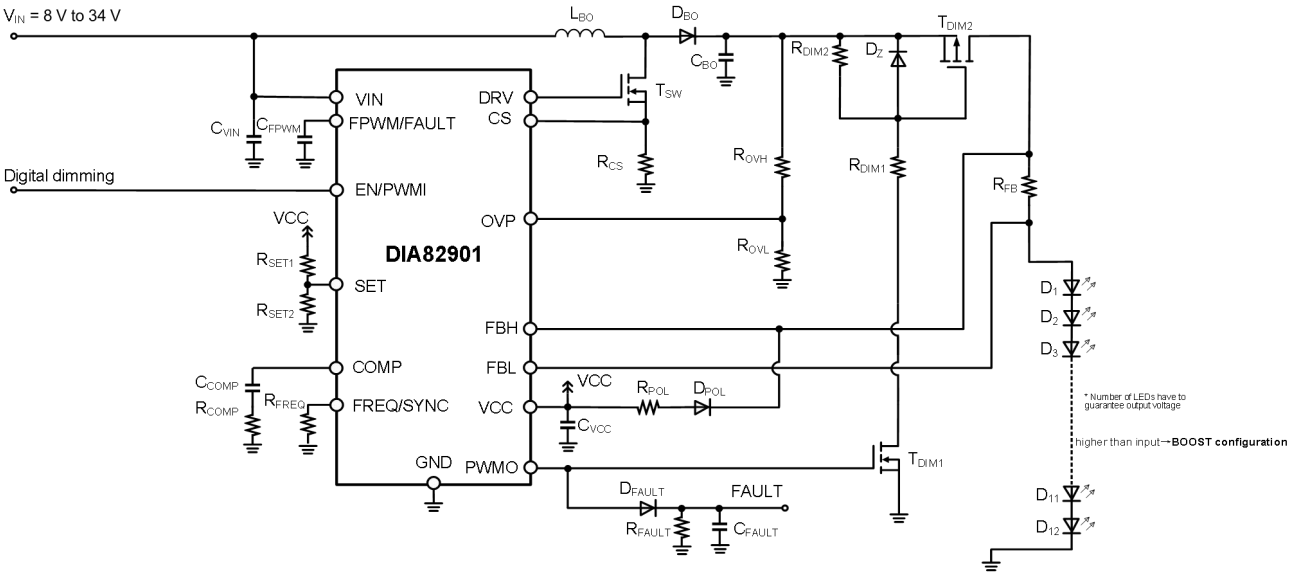


Figure 25. Boost to ground using digital dimming application circuit - B2G (Boost configuration)

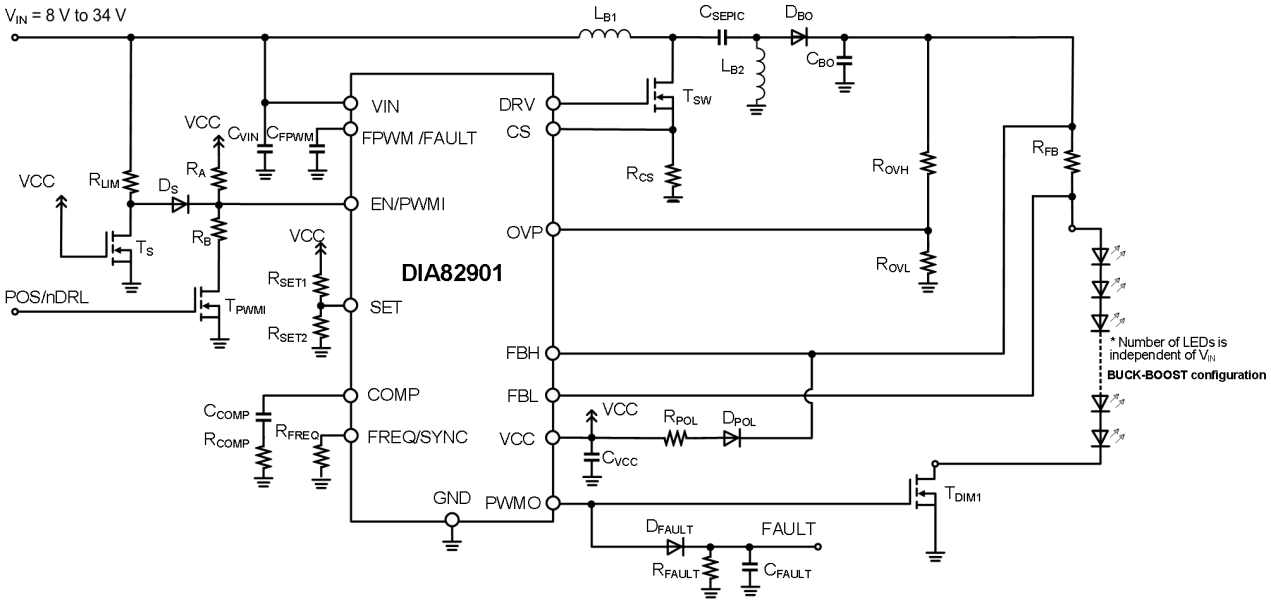


Figure 26. SEPIC using embedded PWM engine application circuit (Buck-Boost configuration)

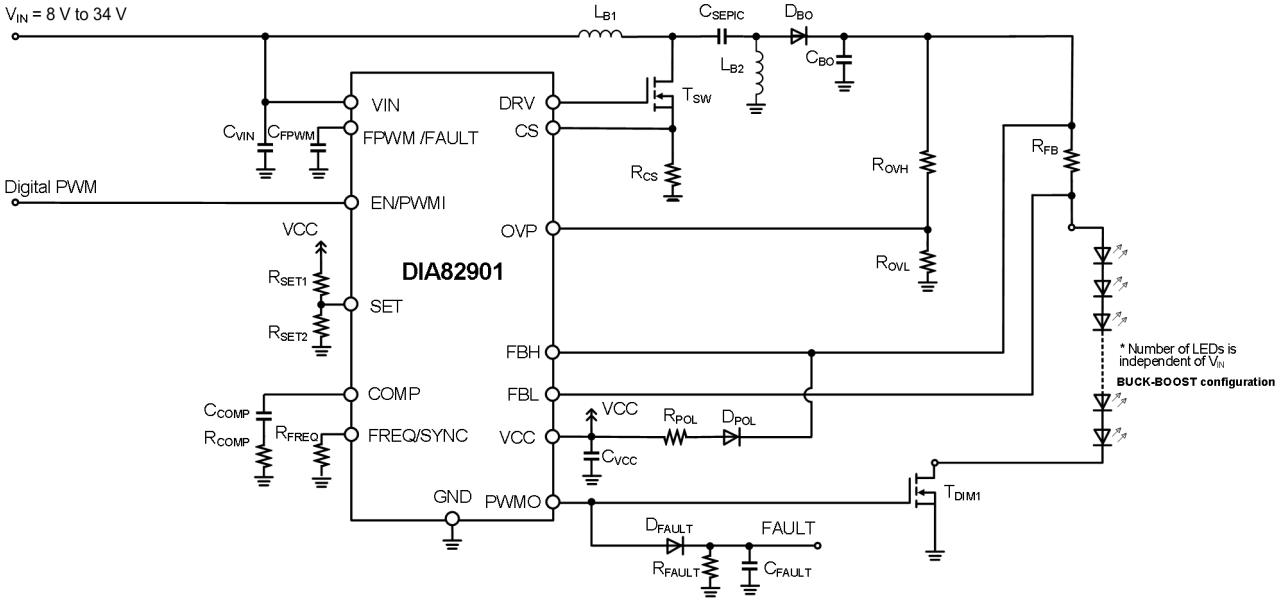


Figure 27. SEPIC using digital dimming application circuit (Buck-Boost configuration)

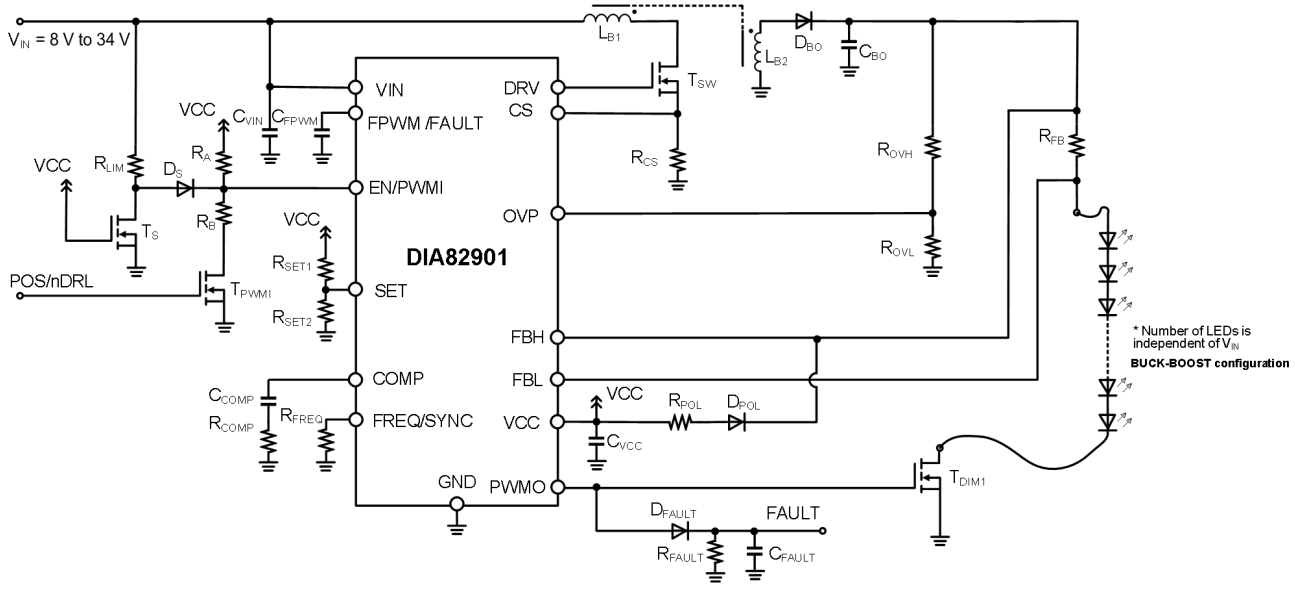


Figure 28. Flyback using embedded PWM engine application circuit (Buck-Boost configuration)

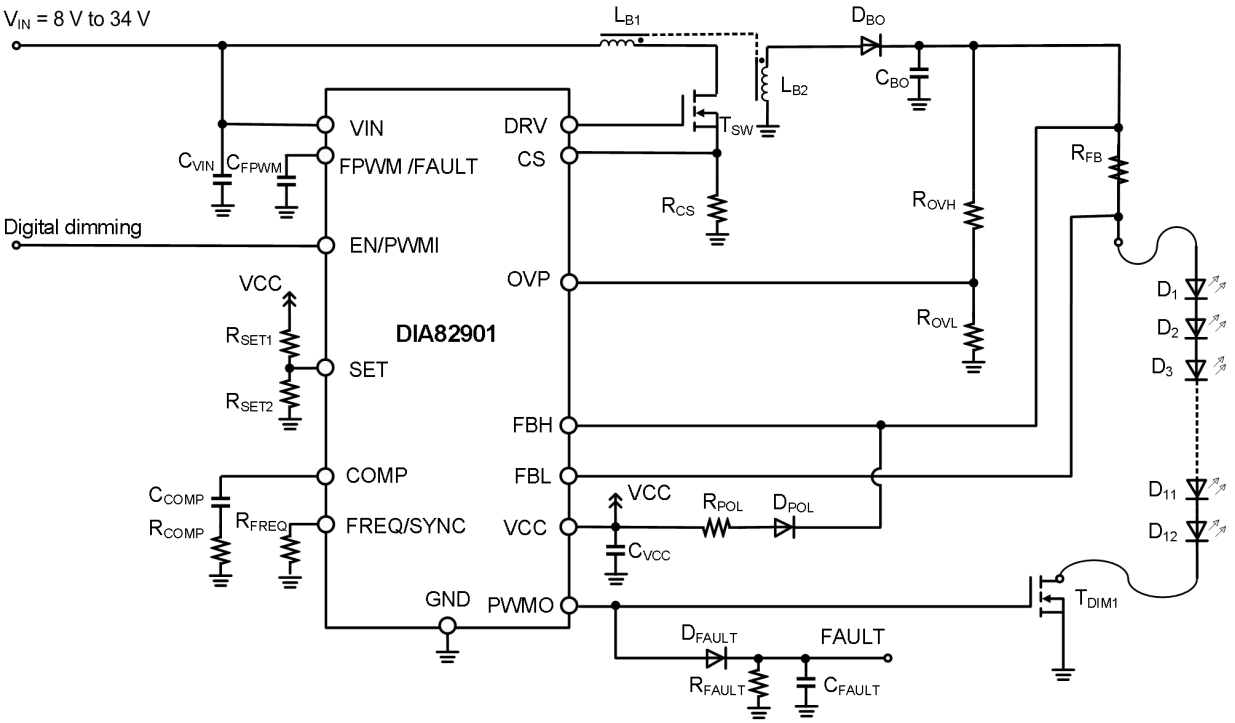


Figure 29. Flyback using digital dimming application circuit (Buck-Boost configuration)

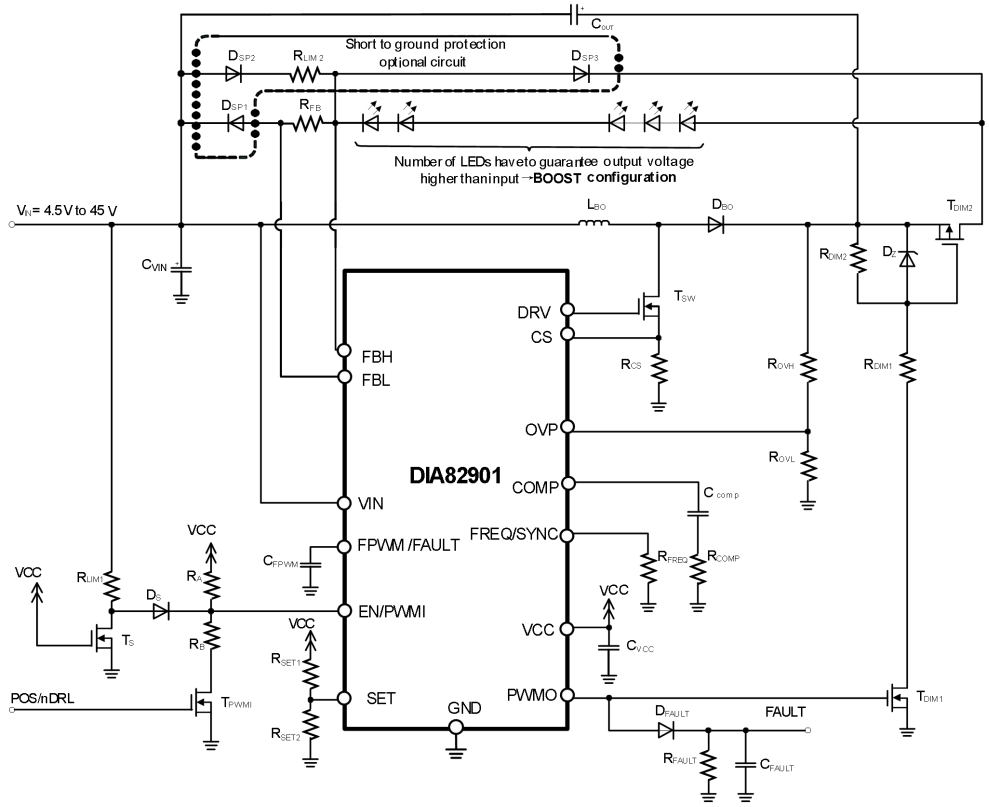


Figure 30. Boost to battery using embedded PWM engine application circuit - B2B (Buck-Boost configuration)

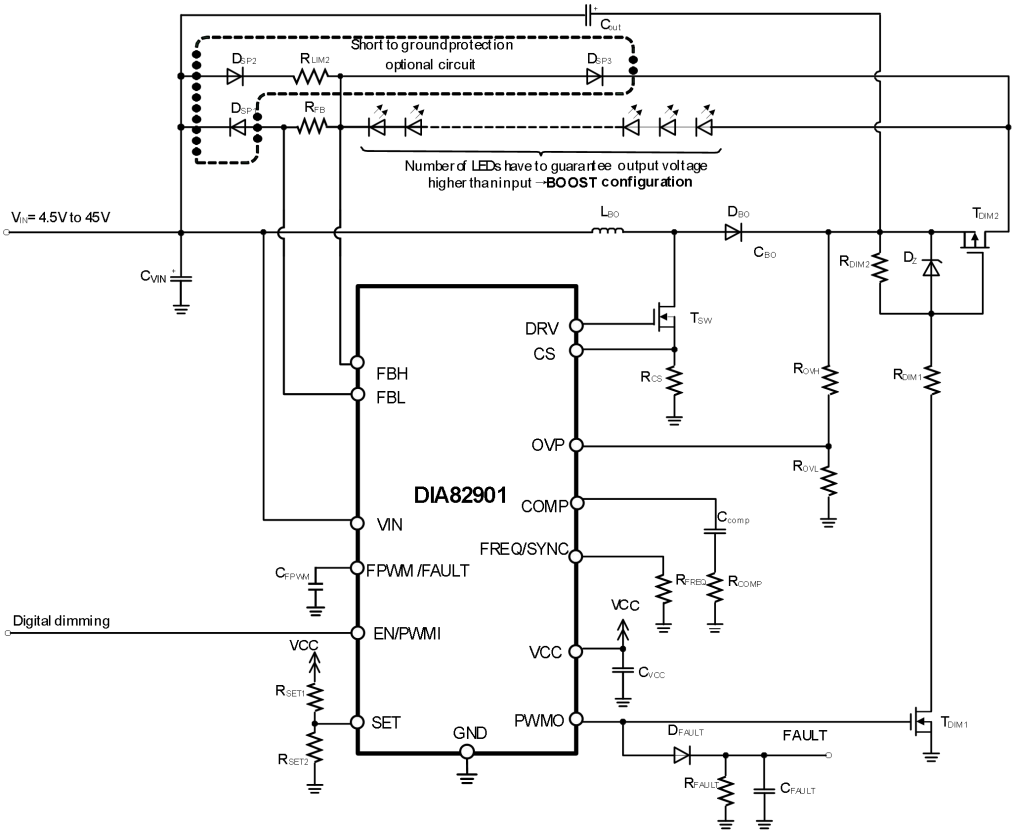


Figure 31. Boost to battery using digital dimming application circuit - B2B (Buck-Boost configuration)

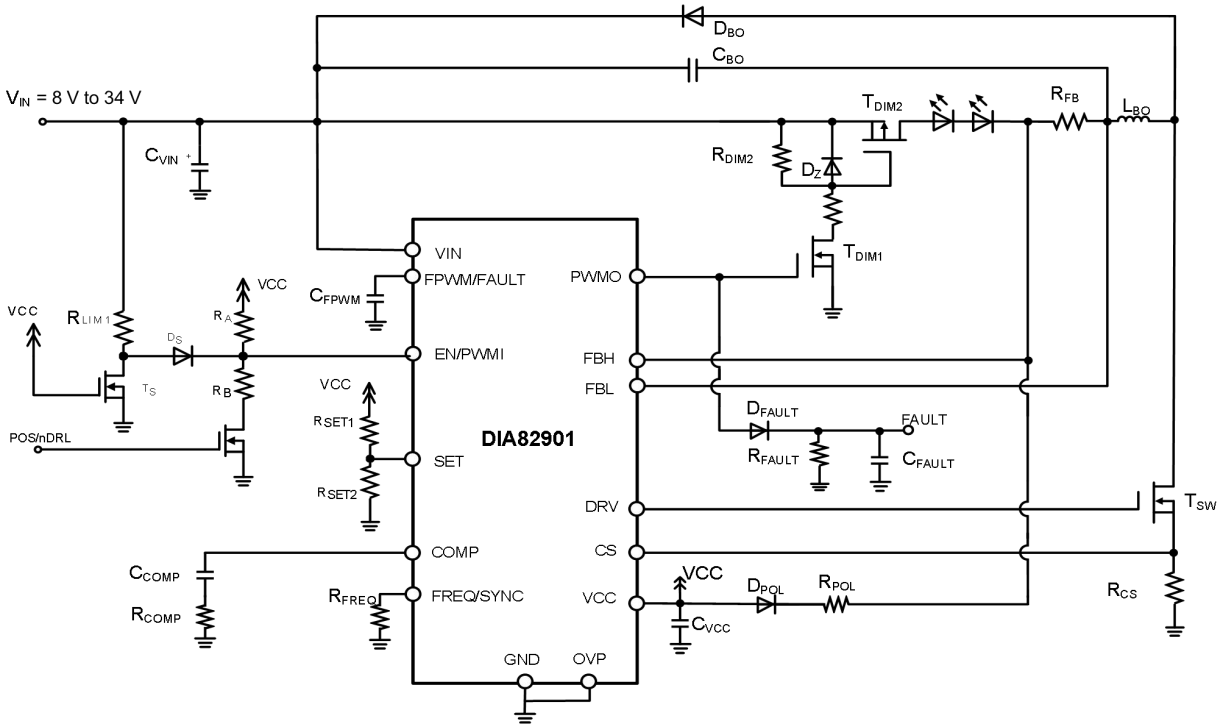


Figure 32. Buck using embedded PWM application circuit

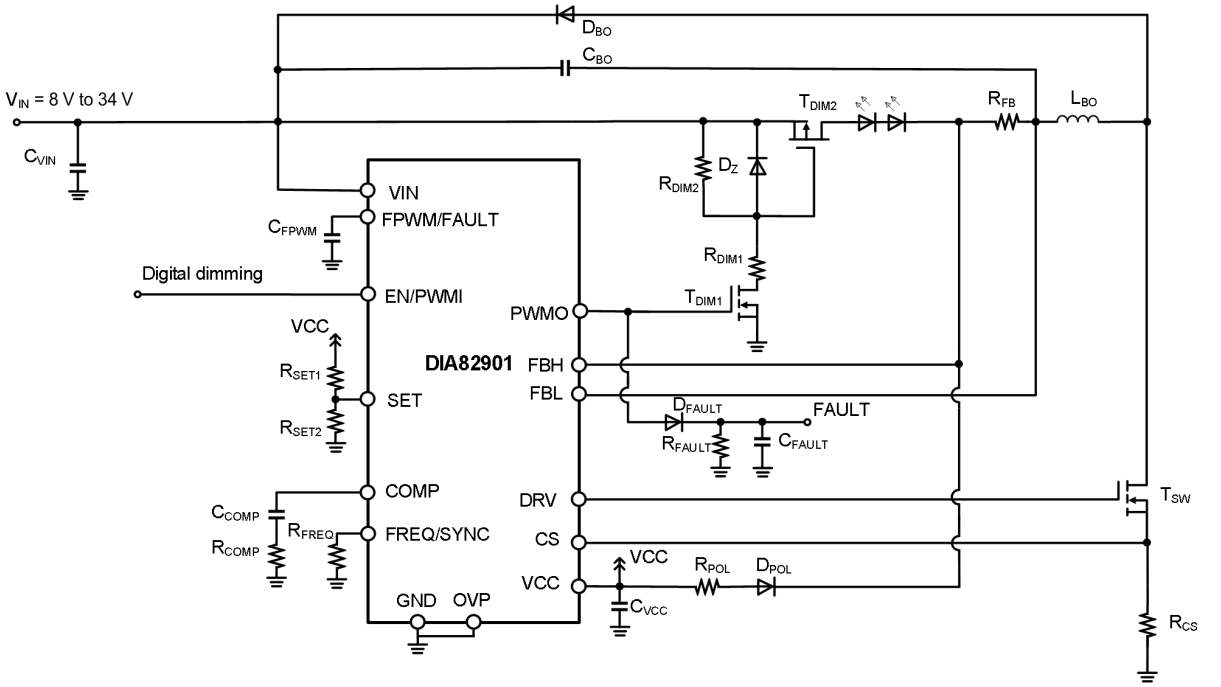


Figure 33. Buck using digital dimming application circuit

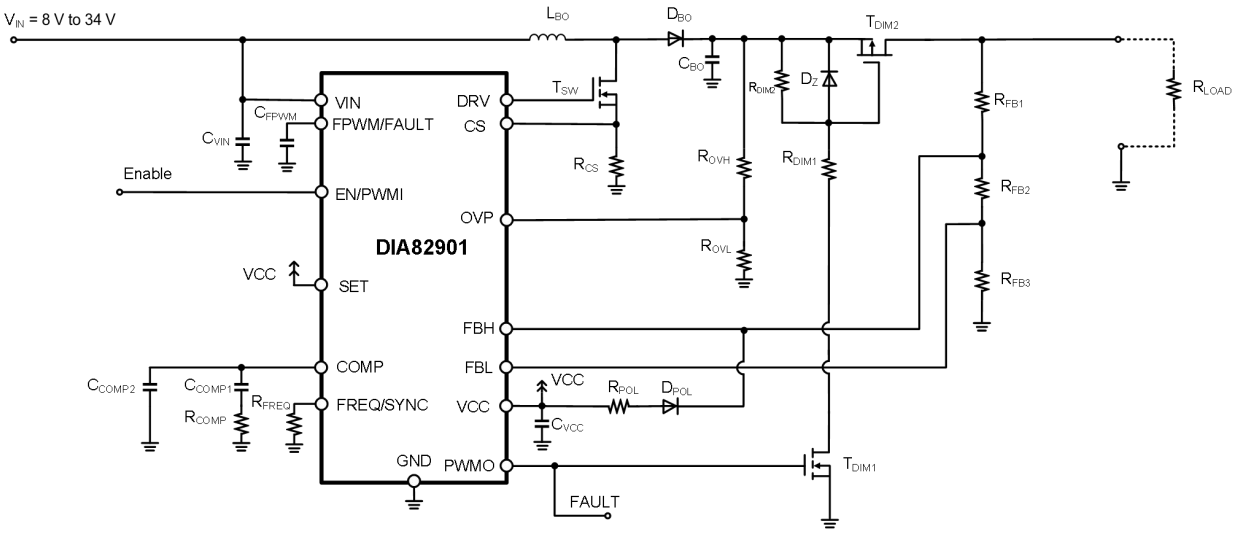


Figure 34. Boost voltage application circuit

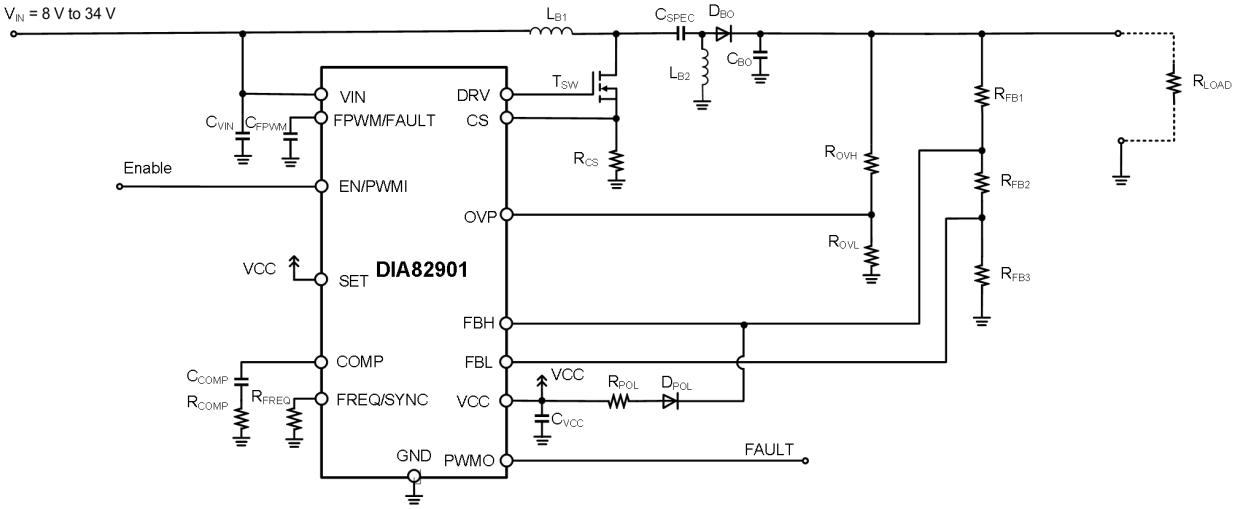


Figure 35. SEPIC voltage application circuit

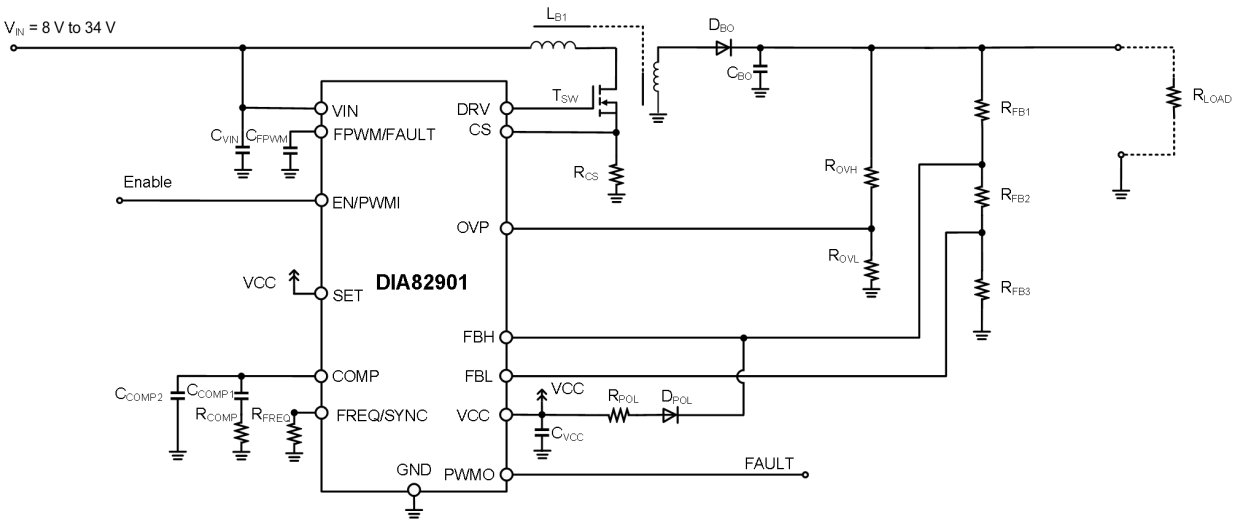
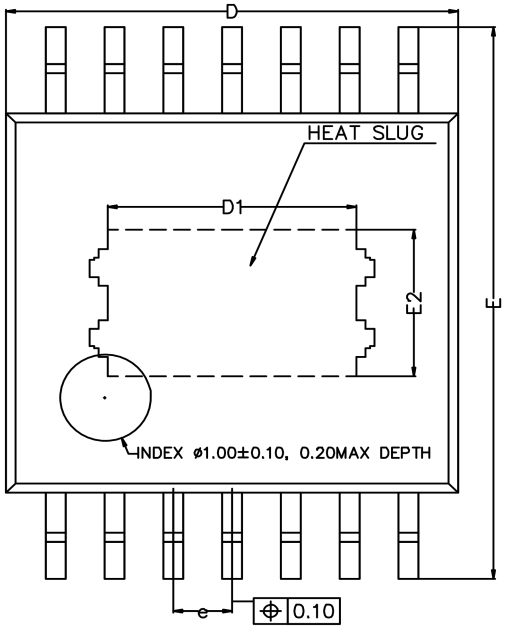
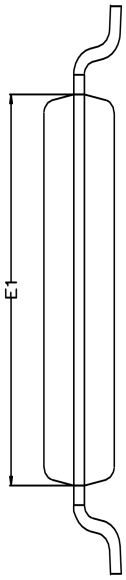
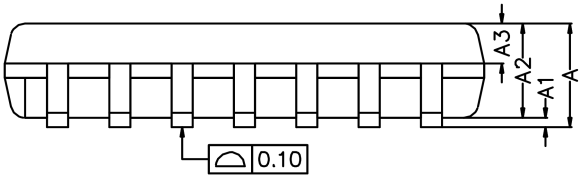


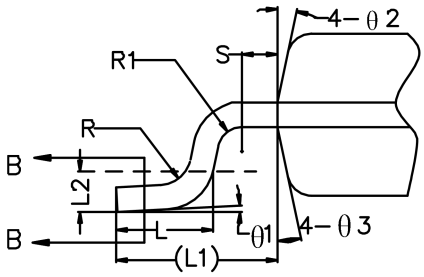
Figure 36. Flyback voltage application circuit

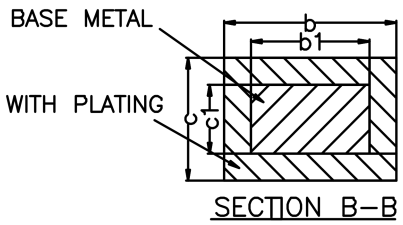
10. Physical Dimensions: EP-TSSOP14











Common Dimensions (Units of measure = Millimeters)			
Symbol	**Min**	**Nom**	**Max**
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.15	-	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
D1	2.65	2.75	2.85
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	1.60	1.70	1.80
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

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