DIO6145

5.5V, 6A, 1.2MHz, High-Efficiency COT Synchronous Step-Down Converter

Features

- Operating Input Range: 2.8V to 5.5V
- Quiescent Current: 40μA
- Up to 6A Output Current
- Fixed Switching Frequency: 1.2MHz
- Adjustable Output from 0.6V
- 700μs Internal SS Time with Pre-Bias Startup
- 20mΩ and 12mΩ Internal Power MOSFETs
- Output discharge resistance: 600Ω
- 100% Duty Cycle in Dropout
- 1% Feedback Accuracy
- External Mode Control
- External VCON Control
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Thermal Shutdown
- Package: QFN2*3-12

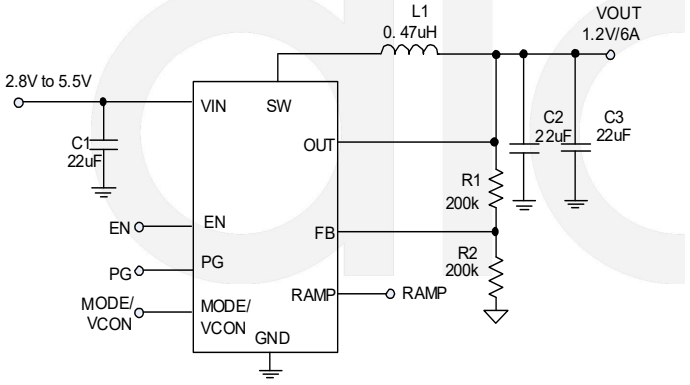
Descriptions

The DIO6145 is a step-down DCDC converter with power MOSFETs integrated. It is able to provide continuous output current up to 6A. The output voltage can be regulated as low as below 0.6V. It also offers various protection scheme such as current-limiting and thermal shutdown. Optimized COT architecture (Constant on Time) allows both fast transient response and loop stability. Housed in a small flip-chip based QFN2*3-12 package, DIO6145 requires minimal external components to implement 6A output capability with superior thermal performance.

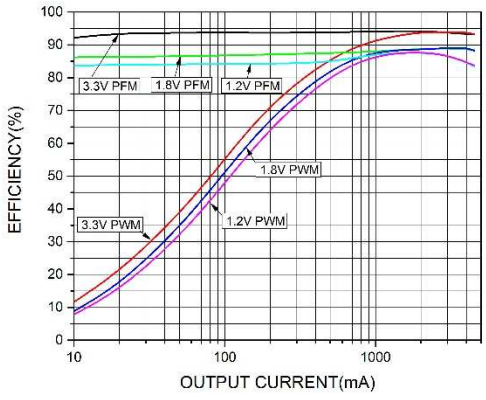
Applications

- Mobile or Battery-Powered Devices
- Storage (SSD, HDD)

Recommended Application



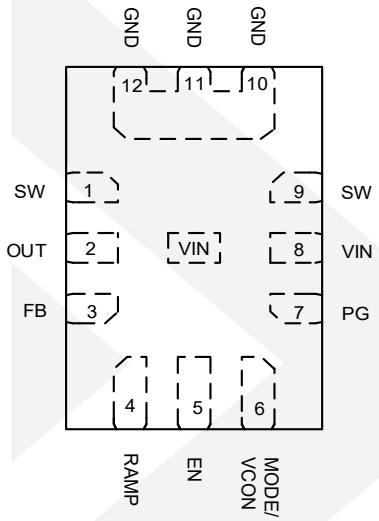
Efficiency
V_{IN}=5V



Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO6145QN12	DFAD5	Green	-40 to 85°C	QFN2*3-12	Tape & Reel, 3000

Pin Assignments



QFN2*3-12

Figure 1 Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
SW	**Inductor Pin.** This pin connected to the internal high-side and low-side power MOSFET
OUT	**Output Voltage Pin.**
FB	**Feedback Pin.**
RAMP	**External Ramp Pin.** Sets the ramp to optimize the transient performance.
EN	**Enable Pin.** Active High. EN pull down resistance is 1MΩ.
MODE /VCON	**Multi-functional Pin.** 1. PWM and PFM Selection pin. When MODE pin is higher than 1.2V, DIO6145 enters PWM mode. DIO6145 enters into PFM mode while MODE is lower than 0.4V or floating. 2. Analog Voltage Dynamic Regulation function pin. Analog voltage input pin which control output voltage by PWM mode.
PG	**Power Good**. The open-drain output with internal pull-up resistor. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is LOW. From when V_{FB} crosses PG threshold to the state when the PG pin goes HIGH, the delay is about 120μs.
VIN	**Power Input Pin.**
GND	**Ground.**

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage	V_{IN}	6.0	V
	V_{SW}	-0.3 (-3V for <10ns) to 6.0 (8V for <10ns)	V
	V_{EN}	-0.3 to V_{IN}+0.3	V
All Other Pins		-0.3 to 6.0	V
Junction Temperature Range		150	°C
Lead Temperature Range		260	°C
Continuous Power Dissipation (T_A = 25°C)		1.78	W

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
Supply Voltage	V_{IN}	2.8 to 5.5	V
Output Voltage	V_{OUT}	0.6 to 5.5	V
Operating Junction Temperature Range		-40 to 125	°C
Package Thermal Resistance	Θ_{JA}	70	°C/W
	Θ_{JC}	15	

Electrical Characteristics

V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_Q	Supply Current (Quiescent)	V_{IN}=3.6V, V_{EN}=2V, V_{FB}=0.65V		40	60	μA
	Shutdown Current	V_{EN}=0V		0.1	1	μA
	IN Under-Voltage Lockout Threshold		2.4	2.55	2.7	V
	IN Under-Voltage Lockout Hysteresis			300		mV
V_{FB}	Regulated FB Voltage	2.8V<V_{IN}<5.5V	0.594	0.600	0.606	V
	FB Input Current	V_{FB}=0.65V		50		nA
	EN High Threshold		1.6			V
	EN Low Threshold				0.4	V
	EN Input Current	V_{EN}=2V		2		μA
		V_{EN}=0V		0		
t_{SS}	Internal Soft-Start Time (1)			700		μs
R_{DSON_P}	High-Side Switch On-Resistance			20		mΩ
R_{DSON_N}	Low-Side Switch On-Resistance			12		mΩ
	SW Leakage Current			0	1	μA
	High-Side Switch Current Limit	Sourcing	7.3	8.2		A
	Low-Side Switch Current Limit (2)	Sinking, PWM Mode		6		A
		Sinking, PFM Mode		0		
	Oscillator Frequency		0.96	1.2	1.8	MHz
t_{ON_MIN}	Minimum On Time			50		ns
t_{OFF_MIN}	Minimum Off Time			60		ns
PGTH_Hi	PG UV Threshold Rising			0.9		V_{FB}
PGTH_Lo	PG UV Threshold Falling			0.85		V_{FB}
PGTH_Hi	PG OV Threshold Rising			1.15		V_{FB}
PGTH_Lo	PG OV Threshold Falling			1.1		V_{FB}
PG_{TD}	PG Delay			120		μs
	PG Sink Current Capability	Sink 1mA			0.4	V
	PG Internal Pull Up Resistor			500		kΩ
	Thermal Shutdown Threshold (2)			150		°C
	Thermal Shutdown Hysteresis (2)			20		°C
	MODE Forced PWM Threshold	V_{IN}=3.6V, V_{EN}=2V	1.2			V

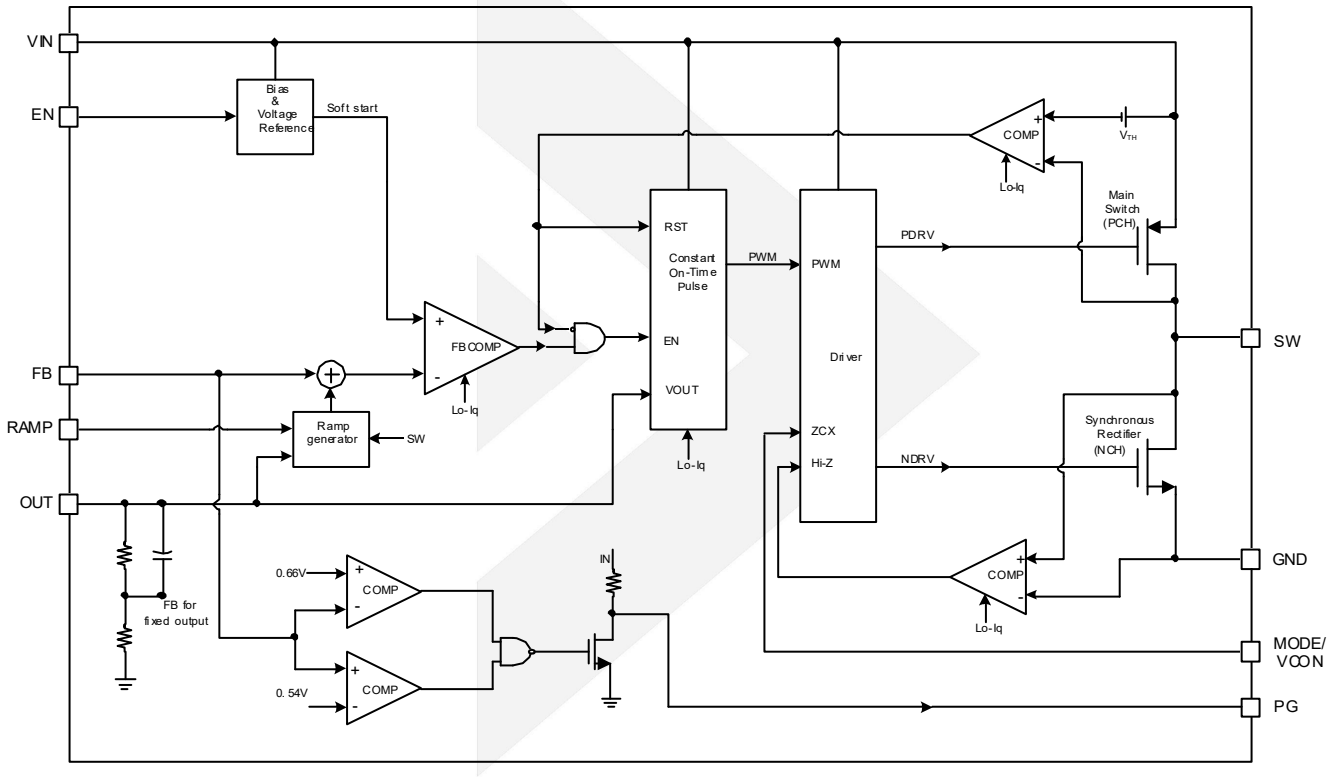
	MODE PFM Threshold	V_{IN}=3.6V, V_{EN}=2V			0.4	V

Note:

(1). Guaranteed by characterization

(2). Guaranteed by design.

Block Diagram

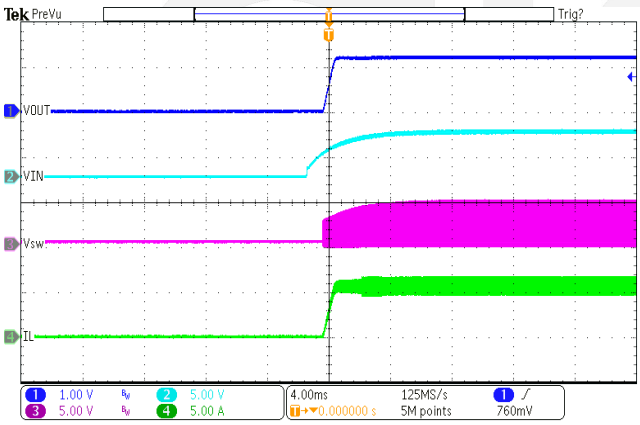


Typical Performance Characteristic

V_{IN}=5V, V_{OUT}=1.2V, L=0.47uH, C_{OUT}=22uFx2, T_A=25℃, unless otherwise specified.

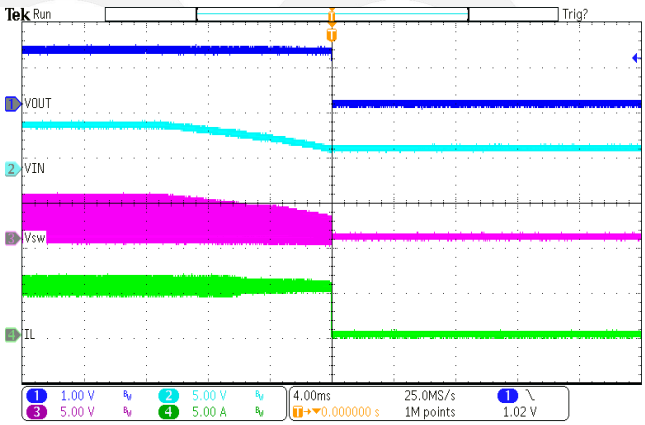
Power on

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6A



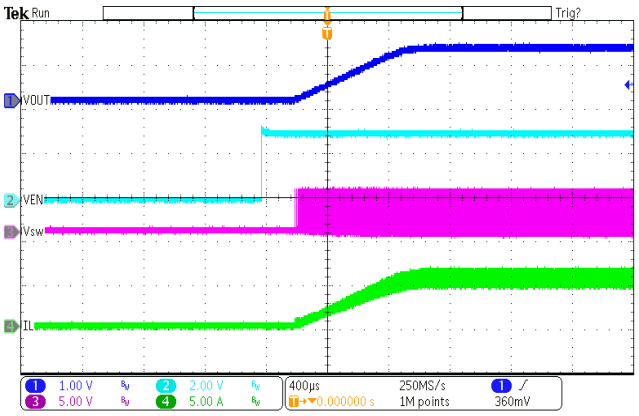
Power off

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6A



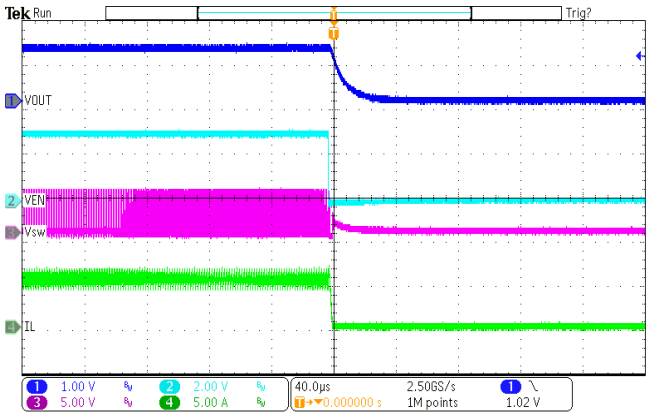
Enable on

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6A



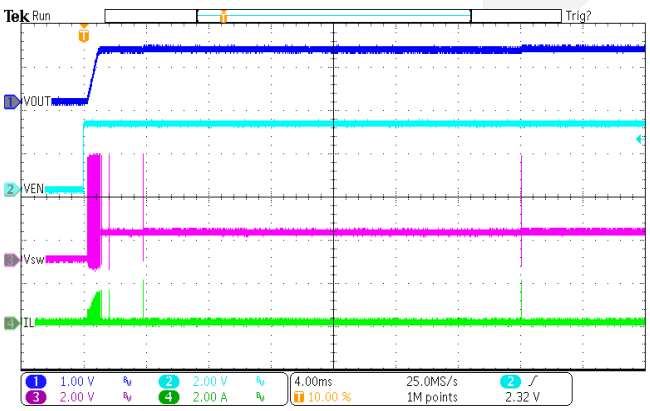
Enable off

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6A



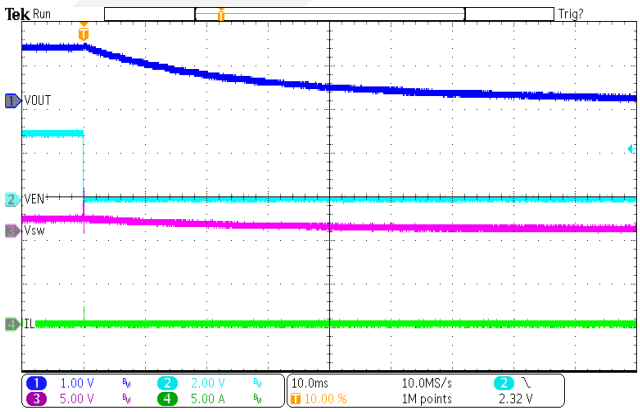
Enable on

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A, PFM



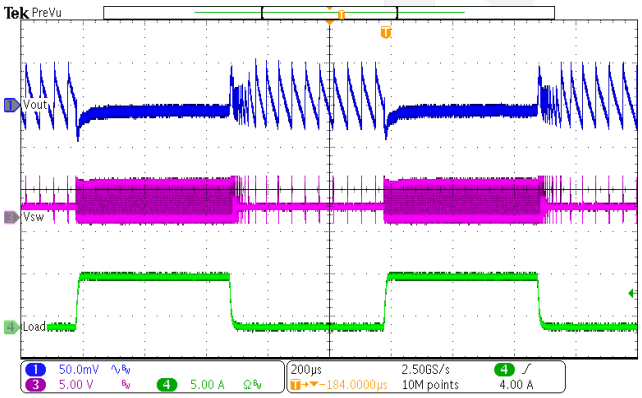
Enable off

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A, PFM



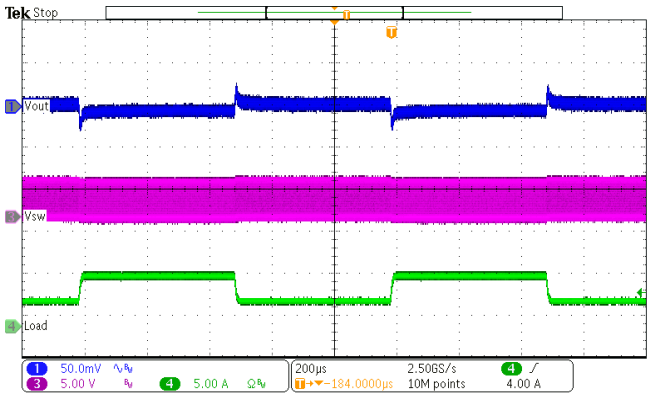
Load transient

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A~6A, PFM



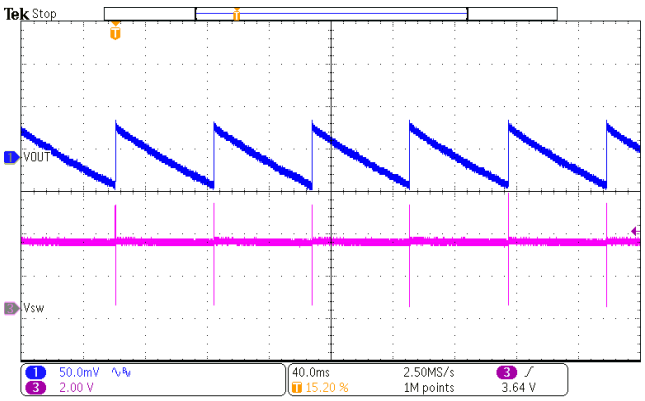
Load transient

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A~6A, PFM



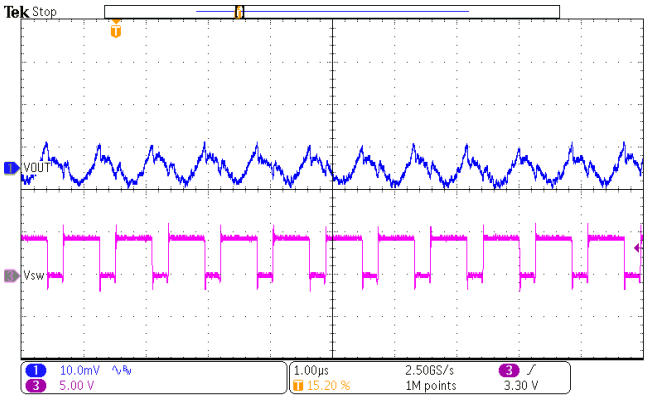
Ripple

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A, PFM



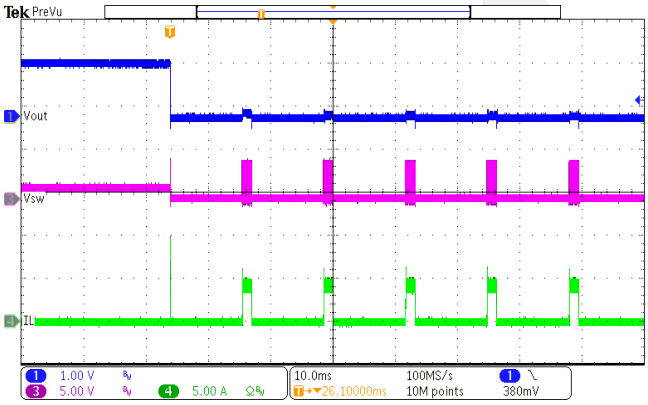
Ripple

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=6A, PWM



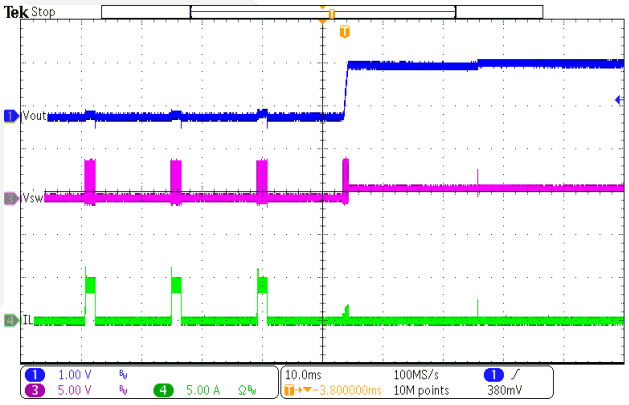
Short Circuit Protection

V_{IN}=5V, V_{OUT}=1.2V, No Load ->short

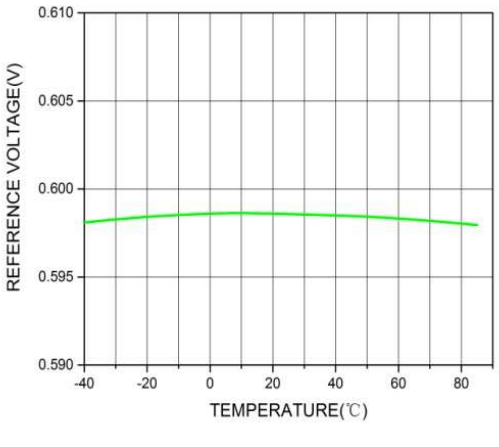


Short Circuit Recovery

V_{IN}=5V, V_{OUT}=1.2V, short -> No load



Reference Voltage vs Temperature



Working Scheme

The DIO6145 uses COT architecture with input voltage feed-forward to stabilize the switching frequency over its full input Voltage range. During light loads, the DIO6145 employs a proprietary control over the low-side MOSFET (LS-FET) and inductor current to improve efficiency.

COT Control

Compared with fixed-frequency PWM control, COT control offers simpler control loop and faster transient response. The DIO6145's input-voltage feed-forward maintains a nearly constant switching frequency across the entire input and output voltage range. Equation below is the estimated on-time of the switching pulse:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} * 0.83us$$

To prevent inductor current runaway during the load transient, the DIO6145 has a fixed minimum off time of 60ns. However, this minimum off time limit does not impact the operation of the DIO6145 in steady-state.

Sleep Mode Operation

DIO6145 adopts sleep-mode to achieve high efficiency under extremely light load condition. In such sleep-mode, most of the circuitry is turned off, except the EA (error amplifier) and the PWM comparator, which results in minimum operation current as shown in Figure 2.

When the loading gets lighter, the ripple of the output voltage is bigger, DIO6145 enters sleep mode. Under sleep-mode situation, the valley of the FB pin voltage is regulated to the internal reference voltage, thus, the average output voltage is slightly higher than the output voltage at DCM or CCM mode. The on-time pulse at sleep mode is about 40% larger than that under DCM or CCM mode. Figure 3 shows the average FB pin voltage relationship with the internal reference at sleep mode.

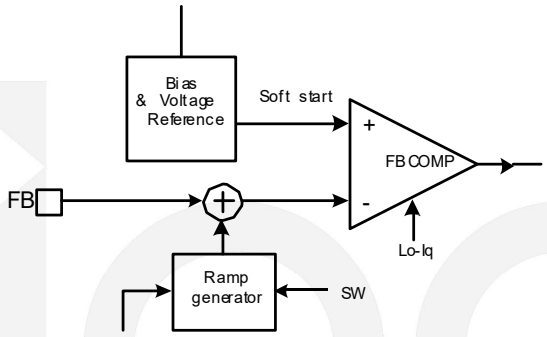


Figure 2 Operation Blocks at Sleep Mode

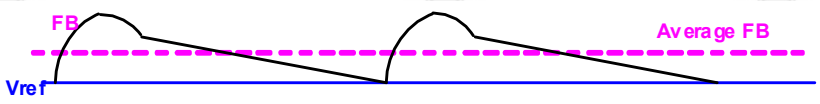


Figure 3 FB Average Voltage at Sleep Mode

Light-Load Mode

During light loads, the DIO6145 uses a proprietary control scheme to save power and improve efficiency: There is a zero current cross circuit to detect if the inductor current starts to reverse. LS-FET turns off immediately when the inductor current starts to reverse and trigger the ZCD in discontinuous conduction mode (DCM) operation.

Considering the internal circuit propagation time, the typical delay is 50ns. It means the inductor current still fall after the ZCD is trigger in this delay. If the inductor current falling slew rate is fast (V_{OUT} voltage is high or close to V_{IN}), the low side MOSFET is turned off and inductor current may be negative. This phenomena will cause DIO6145 not to enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than100ns. For example, V_{IN} is 3.6V and V_O is 3.3V, the off time in CCM is 70ns. It is difficult to enter DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

Enabled Situation

When the input voltage exceeds the under- voltage lockout (UVLO) threshold—typically 2.55V—the DIO6145 can be enabled by pulling the EN pin above 1.6V. Leaving EN pin floating or grounded will disable the DIO6145. There is an internal 1MΩ resistor from the EN pin to ground.

Mode Selection and Analog Voltage Dynamic Regulation

DIO6145 offers programmable PWM and PFM work mode. When MODE/VCON pin is more than 1.2V, DIO6145 enters PWM mode. When MODE/VCON pin is lower than 0.4V or floating, DIO6145 enters PFM mode. PFM mode can achieve high efficiency by light-load operation described above. PWM mode can keep constant switch frequency and smaller V_O ripple, but it has lower efficiency at light load.

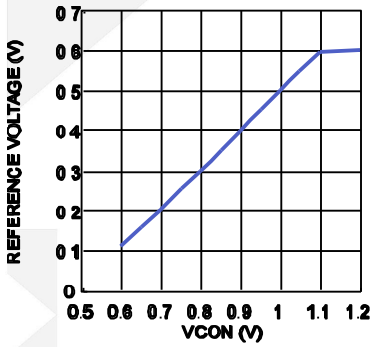


Figure 4 Reference Voltage change with VCON

DIO6145 can dynamic regulate output voltage by MODE/VCON pin to meet some situation need change output voltage directly. When MODE/VCON pin get an appropriate voltage value (from 0.6V to 1.1V), DIO6145 will work with PWM mode and internal reference voltage changes smoothly to achieve a new output voltage without changing external resistor divider, as Figure 4. When VCON function is enabled, set Ref voltage from 0.35V to 0.6V, the accuracy is 3% typically. When set Ref voltage from 0.1V to 0.35V, the accuracy is 10% typically. Detail Ref voltage calculation formula such as below:

$$\mathrm{Re}\, f(V)=0.985*VCON(V)-0.486$$

Soft-Start Details

The DIO6145 has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft- start time is typically about 700μs.

Pre-Bias Startup

The DIO6145 can start up with a pre-bias output voltage. If the internal SS voltage is lower than the FB voltage, the HS-FET and LS-FET remain off until the SS voltage crosses the FB voltage.

Power-Good Indicator

The DIO6145 has an open drain with a 500kΩ pull-up resistor as a power-good (PG) indication. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level. Otherwise the PG pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum R_{DSON} of less than 100Ω.

Current Limit

The DIO6145 has the 8.2A current limit for the HS-FET. When the HS-FET hits its current limit, the DIO6145 enters hiccup mode until the current drops to prevent the inductor current from rising and possibly damaging the components.

Short Circuit Protection and Recovery

The DIO6145 enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short circuit by entering hiccup mode. In SCP, the DIO6145 disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after soft-start ends, the DIO6145 repeats this operation until the short circuit ceases and output rises back to regulation level.

100% Duty Cycle Mode

When the input voltage reduces and is lower than the regulation output voltage, the output voltage drops, and the on time increases. Further reducing the input voltage drives the DIO6145 into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the loading current times the R_{DSON} composed by the high-side switch and inductor.

Application Information

Component Selection

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic).Select the feedback resistor R1 which considers reducing V_{OUT} leakage current, typically between 40kΩ to 200kΩ. There is not strict requirement on feedback resistor. R1>10kΩ is reasoned for some application. R2 can be gotten below then:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1}$$

The feedback circuit is shown as Figure 5:

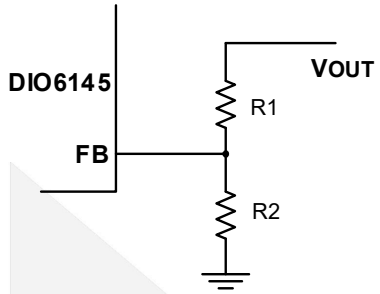


Figure 5 Feedback Network

Table 1 lists the recommended resistors values for common output voltages:

Table 1 Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

In order to achieve high efficiency at light load, a low value inductor such as 0.47μH is recommended for most applications. For highest efficiency, chose an inductor with a DC resistance less than 30mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*\triangle I_L*f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\triangle I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small a 22μF capacitor is sufficient. For higher output system stability.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst case condition occurs at V_{IN} =2V_{OUT}, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1μF), placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\triangle V_{IN} = \frac{I_{LOAD}}{f_S * C1} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})$$

Selecting the Output Capacitor

The output capacitor stabilizes the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to limit the output voltage ripple. Estimate the output voltage ripple as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * f_S * C2})$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{8 * f_S^2 * L_1 * C2} * (1 - \frac{V_{OUT}}{V_{IN}})$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. For DIO6145, 2pcs 22uF C_O can satisfy the most application. Add Co can reduce DCM and CCM output ripple effectively. However, a very large C_O may cause light group pulse in sleep mode.

Load Transient Optimization

DIO6145 can add a capacitor (Cc) between ramp pin and output sense pin to improve load transient. The larger Cc value is, the faster load transient respond speed is. A typical Cc 22pF trades off load transient and loop stability, maximum Cc is less than 200pF in case of SW instability issue. Further, DIO6145 internally has optimized compensate block to cover most application. Ramp pin can be floated in normal application.

PCB Layout Recommendation

Proper layout of the switching power supplies is very important, and sometimes critical to make it work properly. Especially, for the high switching converter, if the layout is not carefully done, the regulator could show poor line or load regulation, stability issues.

For DIO6145, the high speed step-down regulator, the input capacitor should be placed as close as possible to the IC pins. As shown in Figure 6, the 0805 size ceramic capacitor is used, please make sure the two ends of the ceramic capacitor be directly connected to PIN 8 (the Power Input Pin) and PIN 10/11/12 (the Power GND Pin).

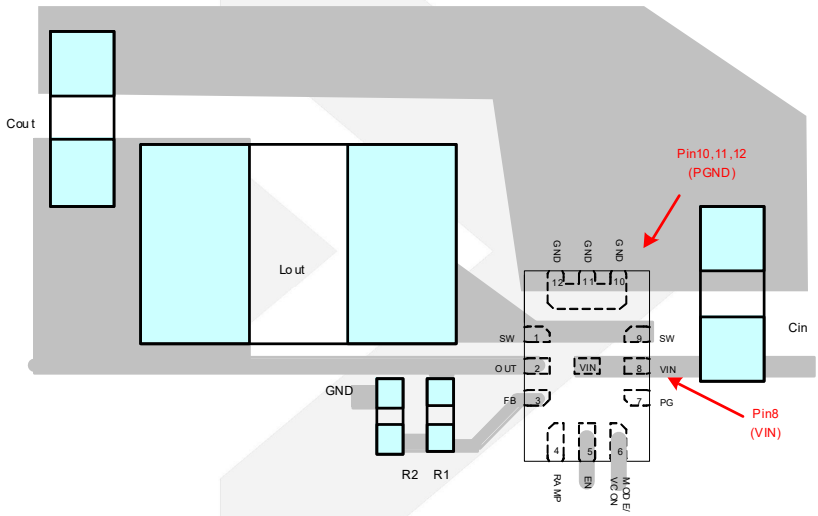


Figure 6 Two ends of Input decoupling Capacitor close to Pin 8 and Pin 10/11/12

Typical Application Circuits

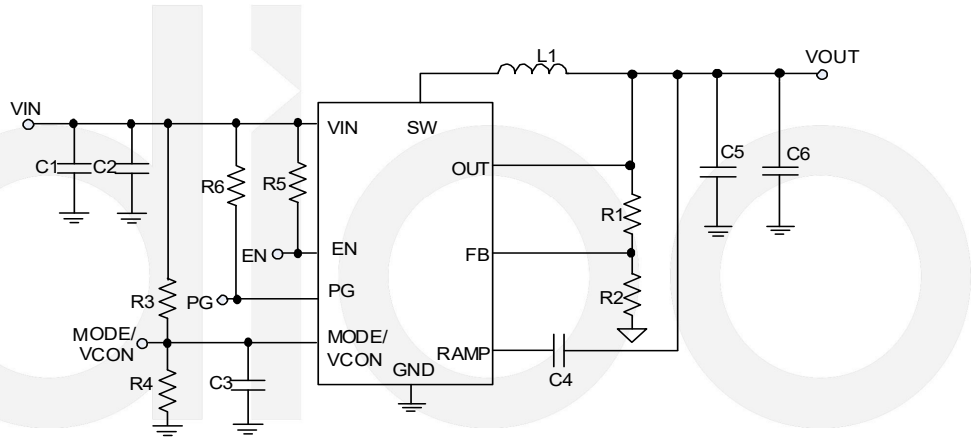


Figure 7 Typical Application Circuit for V_{IN}=5V, I_{OUT}=6A

Note: V_{IN}<3.6V may need more input capacitor.

CONTACT US

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