DIO5000
DP/DM Dual SPDT Switch with 20V Overvoltage Protection

Features

- Operating Voltage Range：2.3V to 5.5V
- Differential 2:1 or 1:2 Switch/Multiplexer
- V_{CC}=0V Powered Off Protection
- Low R_{ON}: 5.5Ω
- BW: 1.5GHz
- C_{ON}: 4.5pF
- Overvoltage Protection (OVP) on Common Pins up to 20V DC
- Temperature Range of -40°C to 85°C
- Package: QFN2*1.5-10 and DQFN1.8*1.4-10

Descriptions

The DIO5000 is a high-speed USB2.0 low-power dual SPDT, analog switch with overvoltage protection. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB2.0 D+/- lines in a USB Type-C system.

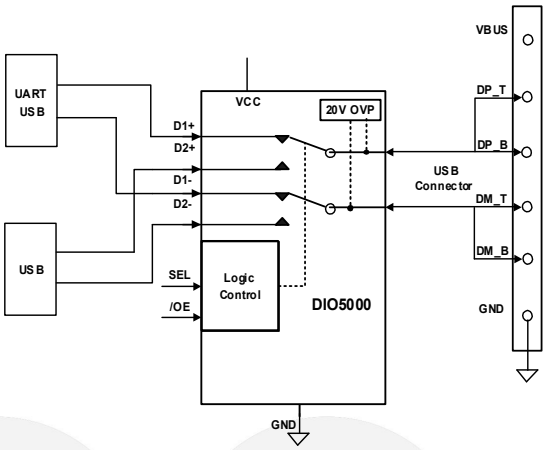
The DIO5000 protects the system components behind the switch with over voltage fault protection up to 20V.

The DIO5000 is available in QFN2*1.5-10 and DQFN1.8*1.4-10 packages, which make it a perfect solution for mobile applications.

Applications

- Mobile
- PC/Notebook
- Tablet
- USB Type-C

Simplified Schematic

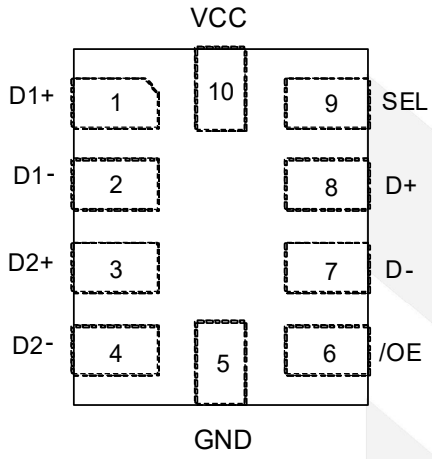


Ordering Information

Order Part Number	Top Marking			T_A	Package	
DIO5000QN10	Fab1	YW5C	Green	-40 to 85°C	QFN2*1.5-10	Tape & Reel,3000
	Fab2	YW5S				
DIO5000LP10	Fab1	YW5C	Green	-40 to 85°C	DQFN1.8*1.4-10	Tape & Reel, 3000
	Fab2	YW5S				

Pin Assignments

QFN2*1.5-10



DQFN1.8*1.4-10

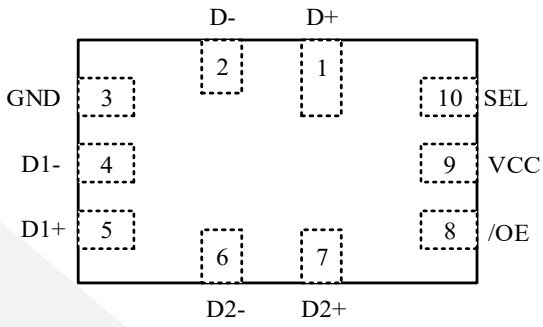


Figure 1. Top View

Pin Description

Pin Name	Direction	Description
D1+	I/O	USB1 Data Link (Differential+)
D1-	I/O	USB1 Data Link (Differential-)
D2+	I/O	USB2 Data Link (Differential+)
D2-	I/O	USB2 Data Link (Differential-)
GND	-	Ground
/OE	I	Output Enable (Active Low)
D-	I/O	Switch Output (Differential-)
D+	I/O	Switch Output (Differential+)
SEL	I	Switch Select (LOW=D+/D- To D1+/D1-, HIGH=D+/D- To D2+/D2-)
VCC	-	Power Supply Pin

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage(1)	-0.5	6	V
$V_{I/O}$	Input /Output DC Voltage (D+,D-)(1)	-0.5	28	V
$V_{I/O}$	Input /Output DC Voltage (D1+/D1-, D2+/D2-) (1)	-0.5	6	V
V_I	Digital Input Voltage (SEL, /OE)	-0.5	6	V
I_K	Input-Output Port Diode Current (D+, D-, D1+, D1-, D2+, D2-) (V_{IN}<0)	-50		mA
I_{IK}	Digital Logic Input Clamp Current (SEL, /OE) (1) (V_I<0)	-50		mA
I_{CC}	Continuous Current Through VCC		100	mA
I_{GND}	Continuous Current Through GND	-100		mA
T_{stg}	Storage Temperature	-65	150	°C

(1) All voltages are with respect to ground, unless otherwise specified.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	2.3 ~ 5.5	V
$V_{I/O\ (D+,\ D-)}$	Analog Input /Output Voltage	0 ~ 20	V
$V_{I/O\ (D1+,\ D1-,\ D2+,\ D2-)}$		0 ~ 3.6	V
V_I	Digital Input Voltage (SEL, /OE)	0 ~ 5.5	V
$I_{I/O\ (D+,D-,D1+,D1-,D2+,D2-)}$	Analog Input /Output Port Continuous Current	-50 ~ 50	mA
I_{OL}	Digital Output Current	3	mA
T_A	Operating Free-Air Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

T_A=-40°C to 85°C, V_{CC}=2.3V to 5.5V, GND=0V, Typical values are at V_{CC}=3.3 V, T_A=25°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
V_{CC}	Power Supply Voltage		2.3		5.5	V
I_{CC}	Active Supply Current	/OE=0V, SEL =0V, 1.8V or V_{CC} $V_{CC}\leqslant$4.4V, 0V<$V_{I/O}$<3.6V		25	35	μA
	Supply Current During OVP Condition	/OE=0V, SEL =0V, 1.8V or V_{CC} $V_{CC}\leqslant$4.4V, $V_{I/O}$>V_{OVP_TH}		25	35	μA
I_{CC_PD}	Standby Powered Down Supply Current	/OE=1.8V or V_{CC}, SEL=0V, 1.8V, or VCC		1.5	10	μA
DC Characteristics						
R_{ON}	ON-State Resistance	$V_{I/O}$=0.4V, I_{SINK}=8mA Refer to ON-State Resistance Figure		5.5	9	Ω
ΔR_{ON}	ON-State Resistance Match Between Channels	$V_{I/O}$=0.4V, I_{SINK}=8mA Refer to ON-State Resistance Figure			0.3	Ω
$R_{ON\ (FLAT)}$	ON-State Resistance Match Flatness	$V_{I/O}$=0V to 0.4V, I_{SINK}=8mA Refer to ON-State Resistance Figure		0.1	0.4	Ω
I_{OFF}	I/O Pin OFF Leakage Current	$V_{D\pm}$=0V or 3.6V, V_{CC}=2.3V to 5.5V $V_{D1\pm}$ or $V_{D2+/-}$=3.6V or 0V, Refer to OFF Leakage Figure	-1	0.5	2	μA
		$V_{D\pm}$=0V or 20V, V_{CC}=2.3V to 5.5V $V_{D1\pm}$ or $V_{D2+/-}$=0V, Refer to OFF Leakage Figure	-1	149	200	μA
I_{ON}	ON Leakage Current	$V_{D\pm}$=0V or 3.6V, $V_{D1\pm}$ and $V_{D2+/-}$=High-Z Refer to ON Leakage Figure	-1	0.5	2	μA
Z_{ON}	ON State Impedance to GND		5	8		MΩ
Digital Characteristics						
V_{IH}	Input Logic High	SEL, /OE	1.4			V
V_{IL}	Input Logic Low	SEL, /OE			0.5	V
I_{IH}	Input High Leakage Current	SEL, /OE=1.8V, V_{CC}	-1	0.5	5	μA
I_{IL}	Input Low Leakage Current	SEL, /OE=0V	-1	0	5	μA
R_{PD}	Internal Pull-Down Resistor On Digital Input Pins			6		MΩ

C_I	Digital Input Capacitance	SEL=0V, 1.8V or VCC, f=1MHz		3.4		pF
Protection						
V_{OVP_TH}	OVP Positive Threshold		4.8	5.1	5.4	V
V_{OVP_HYST}	OVP Threshold Hysteresis		75	230	425	mV
V_{CLAMP_V}	Maximum Voltage To Appear On D1± And D2± Pins During OVP Scenario	$V_{D±}$=0 to 16V t_{RISE} and t_{FALL}(10% to 90%)=100ns R_L=Open, Switch ON or OFF /OE=0V	0		9	V
		$V_{D±}$=0 to 16V t_{RISE} and t_{FALL}(10% to 90 %)=100ns R_L=50Ω, Switch ON or OFF /OE=0V	0		9	V

Dynamic Characteristics

T_A=-40°C to 85°C, V_{CC}=2.3V to 5.5V, GND=0V, Typical values are at V_{CC}=3.3V, T_A=25°C, (unless otherwise noted)

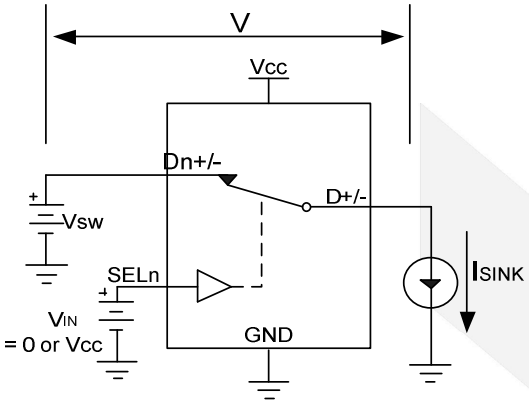
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{OFF}	D+, D- OFF Capacitance	$V_{D+/-}$=0 or 3.3V, /OE=V_{CC} f=240MHz, Switch OFF	1.2	3.5	6.2	pF
C_{ON}	IO Pins ON Capacitance	$V_{D+/-}$=0 or 3.3V, f=240MHz Switch ON	1.4	4.5	6.2	pF
O_{ISO}	OFF Isolation	R_L=50Ω, C_L=5pF, f=240MHz Refer to OFF Isolation Figure Switch OFF		-30		dB
X_{TALK}	Crosstalk	R_L=50Ω, C_L=5pF, f=100kHz Refer to Crosstalk Figure Switch ON		-90		dB
BW	Bandwidth	R_L=50Ω Refer to BW and Insertion Loss Figure Switch ON		1.5		GHz

Timing Requirements

T_A=-40°C to 85°C, V_{CC}=2.3V to 5.5V, GND=0V, Typical values are at V_{CC}=3.3V, T_A=25°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
t_{switch}	Switching Time Between Channels (SEL To Output)	$V_{D+/-}$=0.8V Refer to Tswitch Timing Figure	R_L=50Ω, C_L=5pF, V_{CC}=2.3V to 5.5V		0.6		μs
t_{ON}	Device Turn ON Time (/OE To Output)	$V_{D+/-}$=0.8V Refer to T_{ON} and T_{OFF} Figure			130		μs
t_{OFF}	Device Turn OFF Time (/OE To Output)	$V_{D+/-}$=0.8V Refer to T_{ON} and T_{OFF} Figure			0.05		μs

Application Information



Channel ON, $R_{ON}=V/I_{SINK}$

Figure 2. ON-State Resistance (R_{ON})

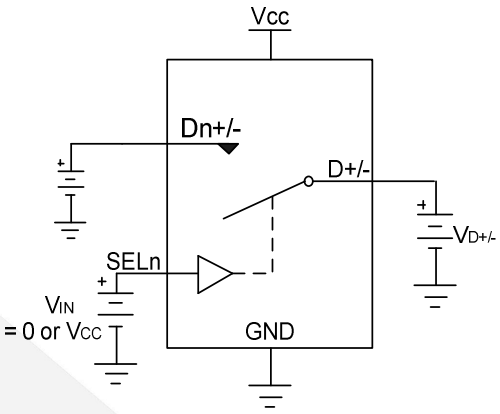


Figure 3. OFF Leakage

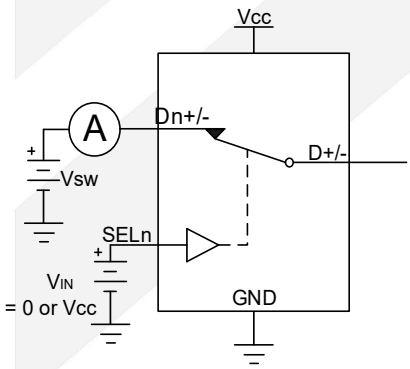
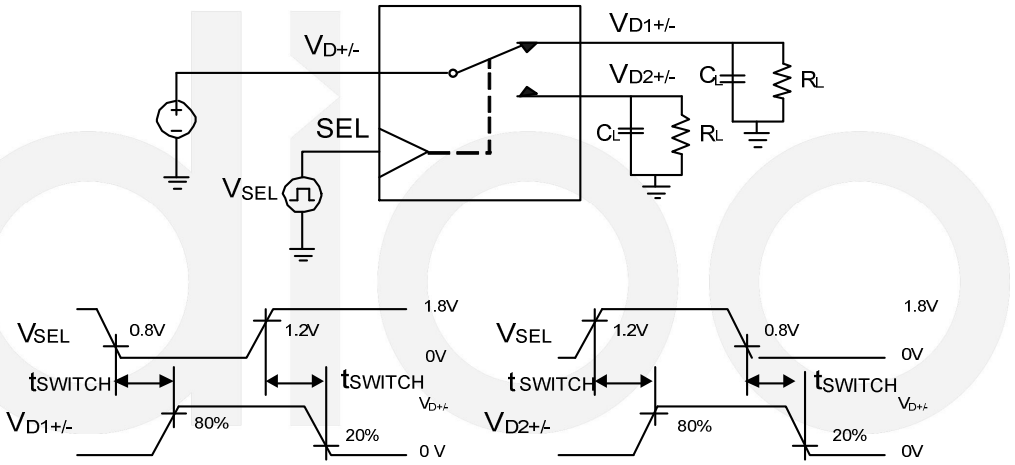


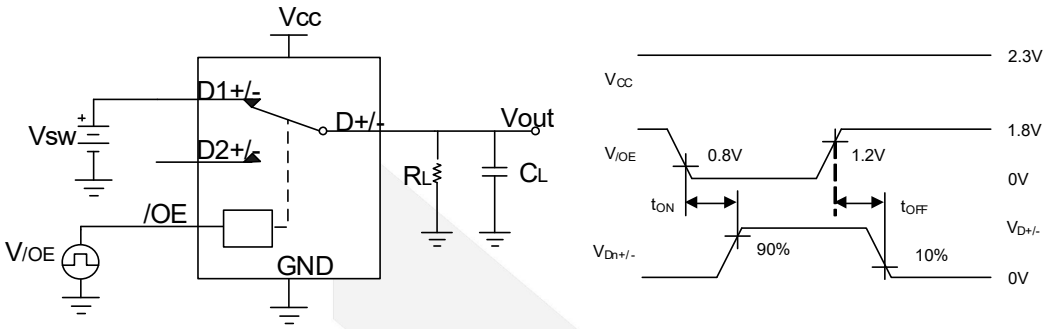
Figure 4. ON Leakage



(1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.

(2) C_L includes probe and jig capacitance.

Figure 5. t_{SWITCH} Timing



(1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.

(2) C_L includes probe and jig capacitance.

Figure 6. t_{ON}, t_{OFF} for /OE

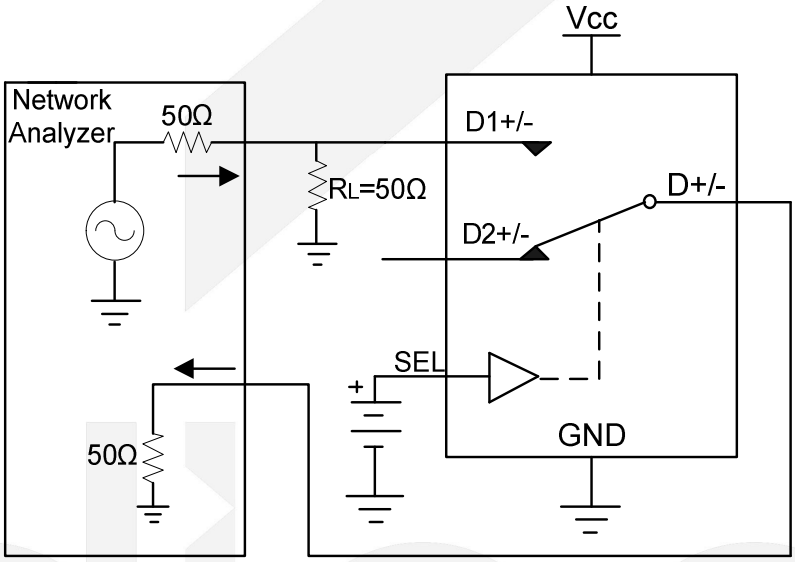


Figure 7. OFF Isolation

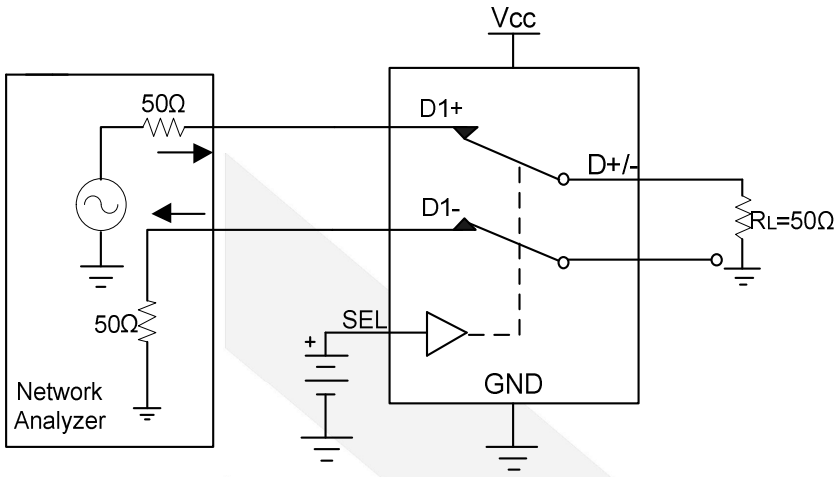


Figure 8. Cross Talk

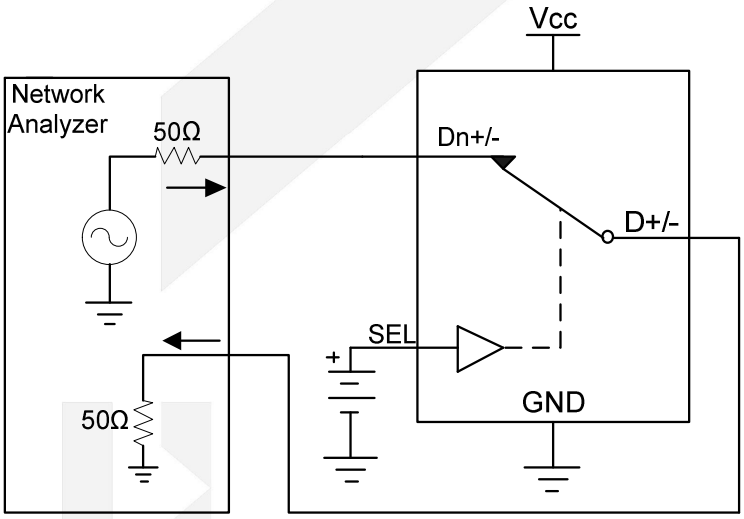
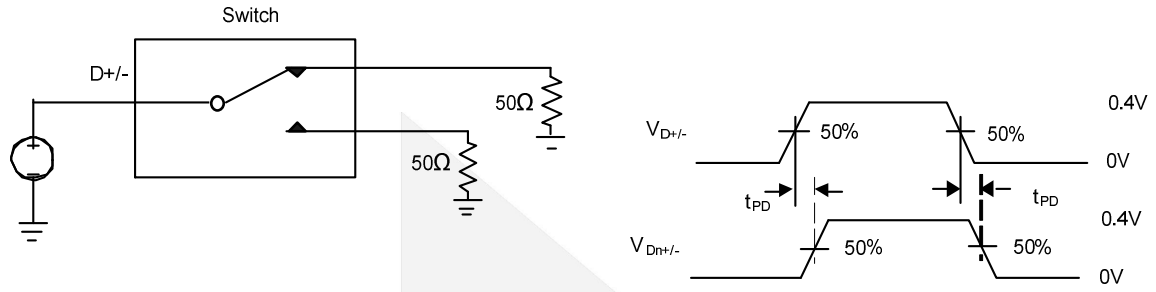


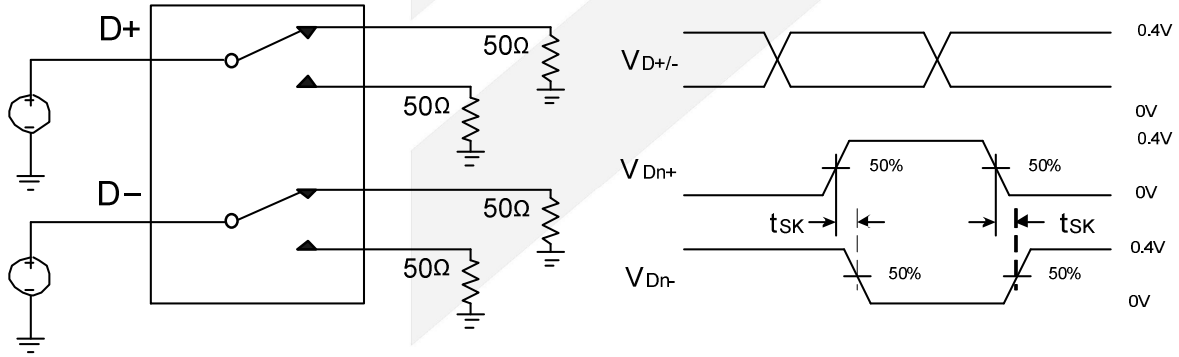
Figure 9. BW and Insertion Loss



(1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.

(2) C_L includes probe and jig capacitance.

Figure 10. t_{PD}



(1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.

(2) C_L includes probe and jig capacitance.

Figure 11. t_{SK}

Detailed Description

Overview

The DIO5000 is a bidirectional low-power dual port, high-speed, USB2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB2.0 D+/- lines in a USB Type-C system as shown in Figure 12.

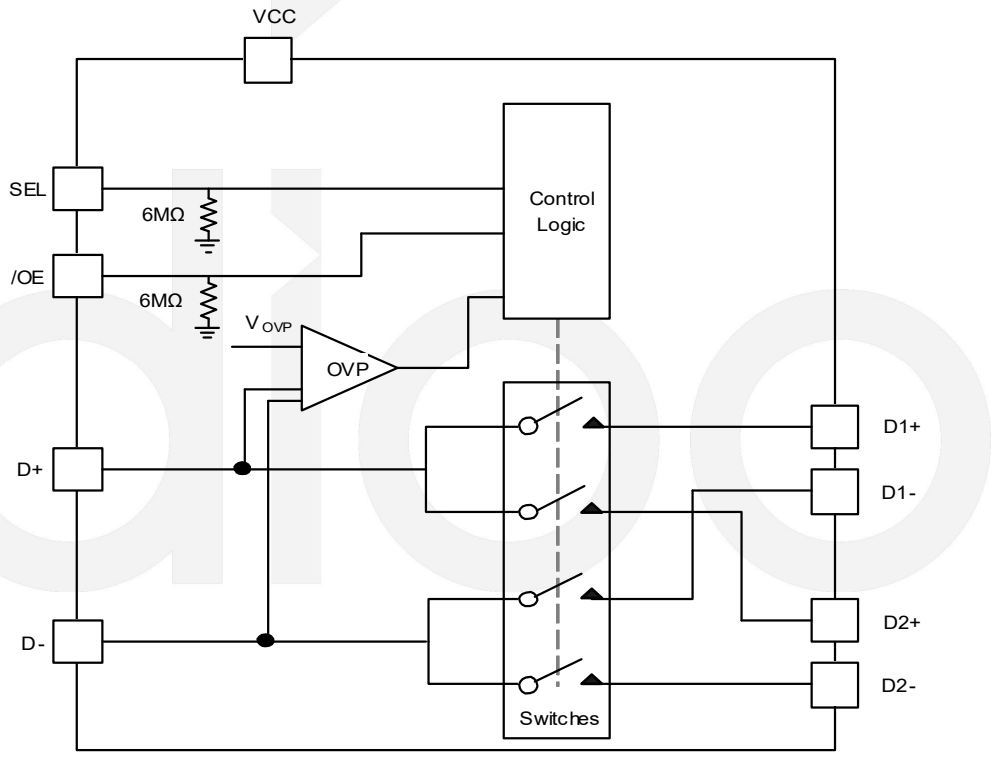
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	+V	CC1	D+	D-	SBU1	+V	RX2-	RX2+	GND
GND	RX1+	RX1-	+V	SBU2	D-	D+	CC2	+V	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

USB3.1 Super speed+ 10Gbps
USB2.0 High speed 480Mbps
Secondary Bus
USB Power Delivery Communication

Figure 12. USB Type-C Connector Pinout

The DIO5000 also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both RON and BW while protecting the system with 0V to 20V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted the D+ and D- pins on the connector.

Functional Block Diagram



Feature Description

Powered-off Protection

When the DIO5000 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the Electrical Specifications.

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

Overvoltage Protection

The OVP of the DIO5000 is designed to protect the system from D+/- shorts to VBUS at the USB and USB Type-C connector. Figure 13 depicts a moisture short that would cause 20V to appear on an existing USB solution that could pass through the device and damage components behind the device.

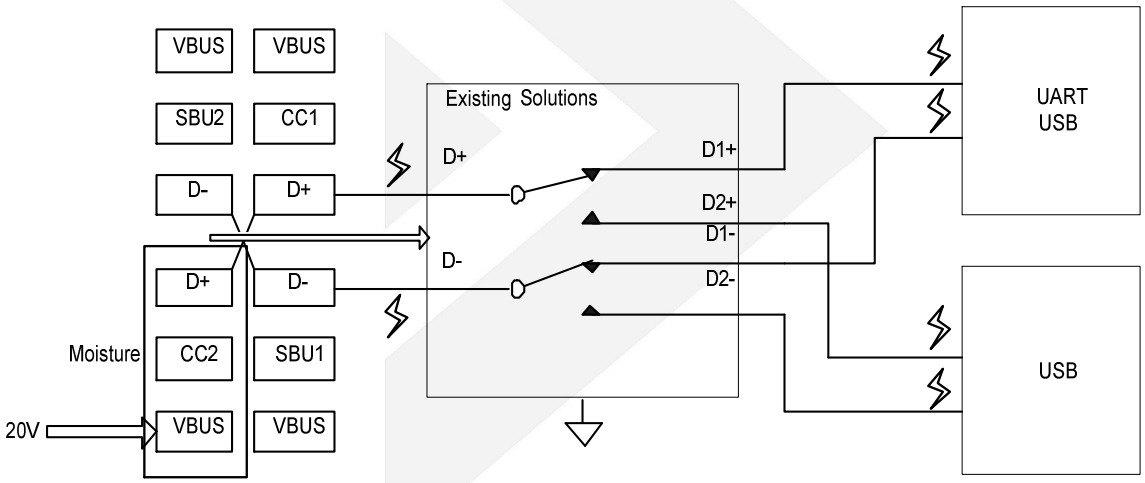


Figure 13. Existing Solution Being Damaged by a Short, 20V

The DIO5000 will open the switches and protect the rest of the system by blocking the 20V as depicted in Figure 14.

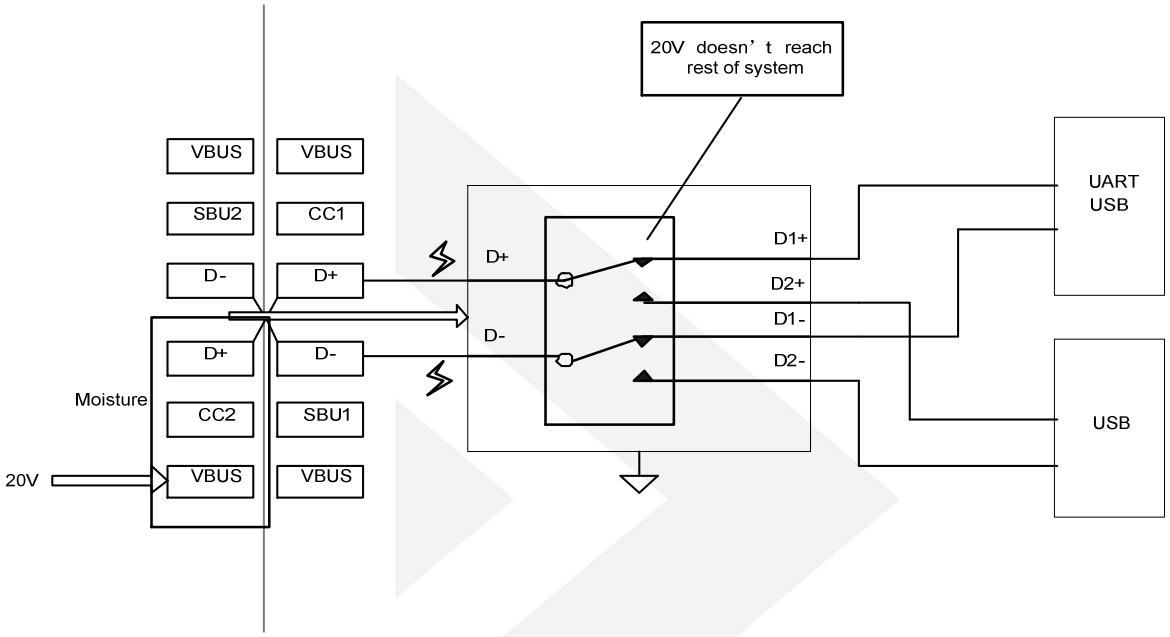


Figure 14. Protecting During a 20V Short

Figure 15 is a waveform showing the voltage on the pins during an over-voltage scenario.

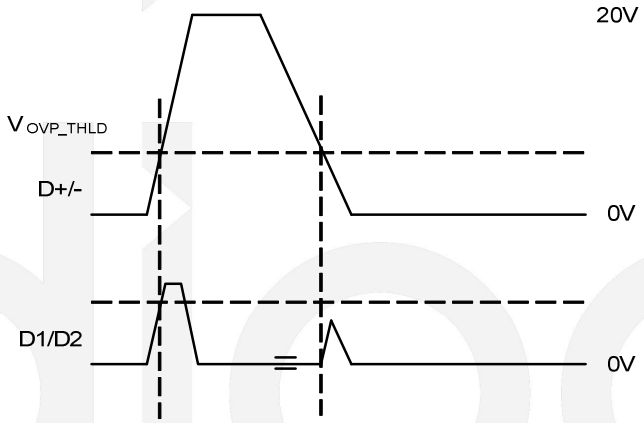


Figure 15. Overvoltage Protection Waveform, 20V

Device Functional Modes

Pin Functions

Table 1. Function Table

/OE	SEL	D- Connection	D+ Connection
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

Application and Implementation

Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The DIO5000 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from on connector to two different locations.

Typical Application

DIO5000 USB/UART switch. The DIO5000 is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The DIO5000 has internal 6MΩ pull-down resistors on SEL and /OE. The pull-down on SEL ensure the D1+/D1- channel is selected by default. The pull-down on /OE enables the switch when power is applied.

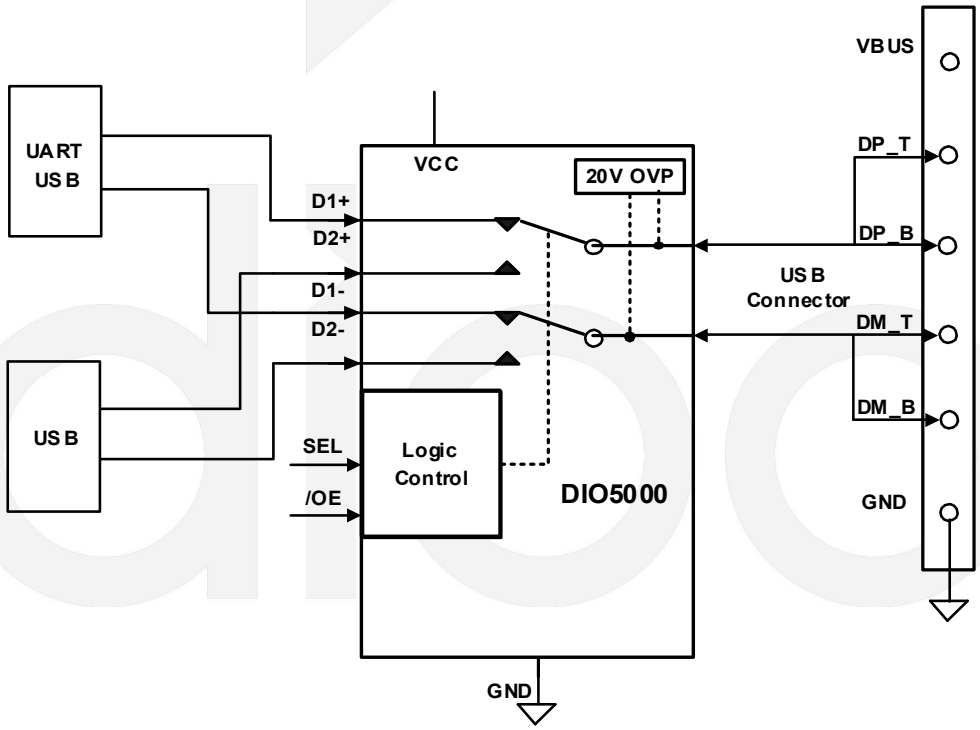


Figure 16. Typical DIO5000 Application

Design Requirements

Design requirements of USB1.0, 1.1, and 2.0 standards must be followed. The DIO5000 has internal 6MΩ pulldown resistors on SEL and /OE, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL ensures the D1+ and D1- channels are selected by default. The internal pull-down resistor on /OE enables the switch when power is applied to VCC.

Detailed Design Procedure

The DIO5000 can be properly operated without any external components. However, DIOO recommends that unused pins must be connected to ground through a 50Ω resistor to prevent signal reflections back into the device. DIOO does recommend a 100nF bypass capacitor placed close to DIO5000 VCC pin.

Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB1.0, 1.1, and 2.0 standards. DIOO recommends placing a 100nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Layout

Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D± traces.
2. The high-speed D± must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D- traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 17.

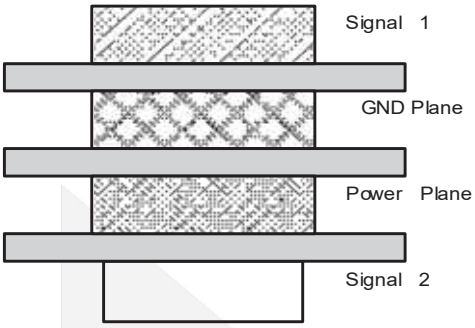


Figure 17. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

CONTACT US

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